ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY CONSORTIUM

2025 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability, and electronic assembly process for consortium Principals. Research ranges from scientific investigations on fundamental material behaviors to engineering topics directly applicable to manufacturing challenges. In every case, the objective is to provide the Principals with meaningful results that enable sustainable packaging and assembly process improvements, maximization of yields and enhanced product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a consortium website (http://www.apl-uic.com/) will be maintained with on-demand content.

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near-term future needs of the electronics manufacturing industry. The research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with the Principals. Longer term reliability evaluation projects may extend into subsequent plan years as needed to complete testing.

The 2025 research plan topics outlined in this document have been categorized into three key thrusts: material evaluation, reliability testing, and assembly process development. The manager and staff will execute the research plan carefully using the resources and facilities of the Advanced Process Laboratory at Universal Instruments along with adjunct university capabilities and faculty expertise as needed. Throughout the year, additional projects may be added as our research interests evolve, lab capabilities develop, and new materials become available.

1. Material Evaluation

Advances in packaging and assembly materials often provide manufacturers with the means to improve process yield and product reliability. The breadth of available materials and complex interactions between materials can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the process windows and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform packaging and assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

1.1 Thermal Interface Materials

The reliable extraction of excess heat from operating semiconductor devices continues to be a challenge in all sectors of the electronics industry. Thermal interface materials (TIMs) are extensively used to dissipate heat from the heat-generating components in electronic packages to prevent them from overheating. The consortium research on this subject has focused on both the first level interface (between die and the lid) materials (TIM1) and the second level interface (between the metal lid and heat sink) materials (TIM2).

Our TIM projects include material processing and application, characterization of the nominal thermal properties (conductivity and interfacial resistance), and investigation of the performance stability in service using different methods. Many of the initiatives within this particular research series may require substantial experimental effort on the design, fabrication and debug of necessary testing apparatus. It is quite common that iterative enhancement must be achieved before arriving at final designs and procedures.

(i) Microstructural Analysis of Solder TIM

Solder TIMs (sTIMs) are indium- or indium-silver-based alloys that can be used as TIM1 materials. They enjoy the advantages of high thermal performance, excellent ductility as well as no pump out after reflow. sTIMs have a much higher thermal conductivity than conventional TIMs. Their high ductility reduces the risk of cracking at the interface keeping the thermal interface resistance low. These properties strongly correlate with the material microstructure, which may change significantly due to intermetallic growth and thermal processing. This project aims to understand the microstructural differences among sTIM alloys as well as the effect of the thermal history especially multiple reflows on the microstructure of each alloy. The sectioning technique developed in the APL will be utilized to characterize the microstructure of soft solder metals.

(ii) Investigation of Solder Thermal Interfaces aged by Accelerated Thermal Cycles

Indium solder thermal interface coupons, comprised of a large silicon die soldered to a plated copper lid, will be vacuum reflowed according to the optimized vacuum reflow profile previously identified for the particular sample configuration of interest. Sample variables will include solder preform composition (0, 3, 10%Ag), solder preform thickness (100, 225, 500 μm), die size, die thickness, and copper lid thickness. All coupons are expected to have some characteristic defect (void) structure despite the process optimization efforts. Coupons will be thermally cycled (0/100 °C and -40/125 °C) and removed at predetermined intervals for x-ray and C-SAM imaging of the defect structure of the solder thermal interface. Select samples will be further measured to understand temperature-induced warpage behaviors.

(iii) IR Imaging for Direct Observation of TIM Stability under Accelerated Power Cycling

The AREA Consortium has developed a test apparatus to monitor the stability of thermal interface layers directly using IR camera imaging. This technique offers the unique capability of in-situ monitoring of the defect formation and growth in TIMs during power cycling. We will evaluate the performance of this newly developed technique on commercially available TIM1 and TIM1.5 compounds including greases, pre-cured gels, phase change materials, as well as alternative TIM options such as liquid metal pastes. This technique requires a TIM layer to be applied between the processing unit (die) and an IR transparent lid (KBr). During the experiment, IR snapshots are continually recorded throughout the test to reveal the onset and growth of defects in the TIM layer. High-resolution optical images are recorded at the end of each test and used to confirm the observations made via the IR camera. In addition, the die temperature is monitored in different areas of the die during the test. Defect formation in the TIM layer may be correlated with the localized increases in the die temperature. An agreement between the IR images, high-resolution optical images and the local die temperature data would validate the applicability of the IR technique to stability analysis of thermal interface compounds.

(iv) Stability Evaluation of TIMs Interfaced with Different Lids

While the IR imaging technique introduced above offers the unique capability of in-situ monitoring of the defect formation and growth in TIMs during accelerated power cycling, the effect of replacing the original copper lid with an IR transparent window is not clear. The KBr window offers a significantly lower thermal conductivity compared to copper. KBr and copper also have different wettability against TIMs that can impact the TIM performance during power cycling. This work intends to compare the performance of different TIMs when interfaced with a copper lid or a KBr window. A thermal test vehicle (TTV) using a CPU package identical to the one used for IR imaging technique (Intel Skylake) will be used to evaluate the performance of different types of common TIMs such as greases, pre-cured gels, phase change materials and liquid metal pastes that have already been analyzed with the IR technique. The die temperature will be monitored in different areas of the die throughout the test. High-resolution acoustic images will be recorded via C-SAM at specific intervals (for example, every 500 cycles) to investigate defect formation in the TIM layer. An agreement between the acoustic images and local die temperature data would confirm the applicability of this analysis technique. Comparing the degradation rates of TIMs with different lids will help us understand the impact of copper lid replacement in the

IR imaging measurements. The results will be used to assess the accuracy and applicability of the IR imaging technique for monitoring the stability of different TIMs.

(v) Capacitive Measurements for TIM2 Stability Analysis

Non-destructive in-situ testing of TIM materials remains a valuable pursuit. Measuring the capacitance of a TIM layer allows for backward calculation of the state of void formation and delamination in the layer relative to the initial condition of the layer. This work will employ a large capacitive measurement board allowing simultaneous measurements of the capacitances of 16 TIM2 samples. The entire board will be subjected to accelerated thermal cycling. The TIM2 material evolution during the lifecycle of the samples will be monitored through periodic capacitive measurements. A power tool for easy, rapid and in-situ TIM stability analysis may be developed by pairing such a capacitive measurement setup with a data logger.

(vi) Spatial Resolution of Thermal Imaging with Laser Flash Analysis

We have previously explored the use of selected area laser heating of heat spreader lids to deduce the presence of voids in the underlying TIM layer by analyzing the transient dissipation of heat into the TIM. Spatial resolution of the technique was found to be quite poor. This project will instead use selected area laser heating of an attached heat spreader while monitoring the heat transmitted through the TIM layer and underlying substrate using an IR imaging camera. The objective is to quantify the spatial resolution of TIM conduction from the transmitted thermal images.

1.2 Solder Alloys

New lead-free solder alloys with varying alloying elements are being routinely proposed by materials suppliers as replacements (improvements) to the standard SAC305 alloy. Industry interests have been in 1) low melting temperature solder alloys to minimize the assembly and reliability challenges posed by temperature-induced component warpage; and 2) high reliability solder alloys with enhanced strength and stability for high power, harsh environment or mission critical applications.

Projects included in this solder alloy research thrust include evaluations of microstructure and mechanical properties of various solder alloys, pastes and surface finishes. The work typically encompasses characterization of both individual solder balls wetted to a surface finish of interest as well as components assembled onto test boards for second-level reliability comparisons through thermal cycling or mechanical testing. The performance of the alternative lead-free solder joints is often compared to that of the common SAC305 alloy or eutectic SnPb, as appropriate.

(i) Reliability Study of Hybrid Solder Joints Formed with Various High Reliability Solder Pastes

Many so-called High Reliability solders, based on modifications to the ubiquitous SAC305 formulation, have been introduced with the promise of improved thermal cycle reliability of solder joints. Most such alloys include solid solution levels of Bi. For the most part, these alloys have not yet been adopted by the

semiconductor packaging industry. BGA components are therefore not yet available with various high reliability solder balls. Early adopters of such high reliability solder alloys are therefore forced to mix these solder pastes with SAC305 spheres in card assembly. Since SAC305 spheres melt during the reflow of the solder pastes, the solder joint mixing is more complete than in previous mixing cases in which only the paste melts, but the strengthening effects of the Bi are dramatically diluted, thereby reducing its reliability benefit. High reliability solder pastes of interest include Cyclomax (SAC-Q), MaxRel, Alpha C10, Senju M58, and Indium Duafuse HR. The reliability of these mixed alloy solder joints will be tested with thermal cycling between -40-125 ^{o}C in a variety of common BGA package types. Paste printing and reflow process optimization trials will be run for all alloys prior to building the final test assemblies.

(ii) Drop Test Evaluation of High Reliability Solder Pastes

Four high reliability solder pastes will be evaluated using SAC305 BGA test vehicles subjected to mechanical shock testing. These alloys are: Cyclomax, Durafuse HR, Rel22, and C10. A fifth high reliability solder paste, Rel61 may also be evaluated if available. Samples will be assembled using standard SAC305 processes and drop tested. SnPb and SAC305 assemblies will also be prepared and evaluated for comparative purposes. Further testing in which the specimens are subjected to constant current stressing prior to drop testing is also planned.

1.3 Sintering Pastes

(i) Pressure Sintering of Copper Sintering Paste

With the proven success of silver sinter interconnects, the industry is now setting its sights on copper sintering as the next logical advancement. Copper sintering offers a more cost-effective solution for high-power applications. However, the high susceptibility of copper to oxidation remains a challenge. Pressure sintering enables the use of larger-than-nanoscale copper, lowering the oxidation tendency, while maintain densification and bonding quality. The AREA Consortium is expanding its footprint in pressure sintering, evaluating the performance of copper pressure-sintered materials across various surface finishes and aging criteria. This work will open a new pathway to develop pressure copper sintering as a pivotal technology in the advanced power electronics packaging.

2. Reliability Testing

The investigations conducted by the AREA Consortium into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. We take a more holistic approach, considering the contributions of the test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to

improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of the test methodology as well.

(i) Effects of Electromigration Pre-Stress on Thermal Cycle Lifetime of LTS

Previous efforts to evaluate the impact of current stress on the thermal cycle lifetime of low temperature solder BGA joints was fraught with experimental difficulties. Only a limited number of test nets could be wired for direct current flow during the thermal cycles. Excessive joule heating of the sample would result if all test nets were exposed to current. All BGA solder joints are however stressed during the environmental thermal cycles of an attached processor module. Attempts to select which nets would fail in thermal cycle such that those could be simultaneously current stressed proved unsuccessful. In this follow-on project, all test nets on BGA assemblies with SnBi solder joints will be uniformly pre-stressed with a high electric current. The pre-stressed samples will then be thermally cycled without a superimposed current flow. This experimental design allows us to investigate the effects of current-induced Bi electromigration in the SnBi alloy on the thermal cycle lifetime of the low-temperature solder joints.

(ii) Effects of Pre-Current Stress on Vibration Fatigue of LTS Joints

In this project, BGA assemblies will be surface-mounted using low-temperature SnBi solder alloys. All test nets on the boards will be uniformly pre-stressed with a high electric current. The pre-stressed samples will then be subjected to vibration test without a superimposed current flow. This project aims to investigate the effects of current-induced Bi electromigration and accumulation on the vibration fatigue of the low-temperature solder joints.

(iii) Shear Strength of Solder Joints Subjected to Temperature and Current Stressing

Solder alloys containing bismuth have demonstrated significant electromigration phenomena when subjected to relatively harsh accelerated conditions, resulting in extremely brittle solder joints. However, actual usage conditions may or may not provide the necessary energy to drive electromigration. This study will evaluate how current stressing influences the mechanical robustness of various solder alloys by comparing the shear strength of 0603 surface mount resistors using realistic stress conditions of 0.33 A and 0.66 A at 75 °C solder joint temperature. Bismuth bearing high-reliability Durafuse HR, and low-melt L29 solder pastes will be evaluated along with SAC305 and SnPb for stress durations believed to represent up to 3 years of operational time.

(iv) Thermal Cycle Reliability Analysis of Cyclomax Solder Joints

Cyclomax is a SAC based solder alloy with 3.3%Bi. Our 2024 research evaluated the reliability of hybrid Cyclomax paste/SAC305 BGA joints and concluded that Cyclomax paste assemblies are comparable to, or often better than, standard SAC305 assemblies. In 2025, additional thermal cycle studies will be carried out to evaluate pure Cyclomax BGA assemblies (i.e. Cyclomax paste/Cyclomax solder ball) using -40 to 125 ^{o}C accelerated thermal cycling and the results will be compared to SnPb and SAC305 assemblies**.**

(v) Drop Test of Current-Stressed L29 Solder Joints

The electromigration evaluation of L29, a low temperature solder containing 58% bismuth using mechanical shock testing will enter the fourth phase of experimentation. In this phase, the solder alloy will be exposed to realistic commercial product operational temperatures with realistic current densities being applied. Specifically, solder joints will be stressed at 0.71 kA/cm^2 and 0.44 kA/cm^2 at temperatures of 55 and 65°C. Drop testing will be performed after various stress durations, which have been calculated to represent 1- and 3-year warranty periods based upon product data provided by an AREA member. SAC305 samples will be tested under similar conditions for comparative analysis.

(vi) Shear Test of High-Reliability Solder Joints in Thermally Aged LED Packages

Many high reliability solder alloys are designed to optimize the thermal cycling capability beyond the SAC performance. For LED products, high reliability solder joints with good mechanic strength are particularly important due to a large CTE mismatch between stiff LEDs and aluminum-clad PCBs. The ability of the solder to retain strength after many hours of use is important as well. Our previous consortium work addressed the shear strength reliability of LEDs with an ImmAg surface finish. This project explores the shear strength of ENEPIG plated LED I/O joints with three different high reliability alloys as well as SAC. The shear strength both before and after accelerated thermal aging at 105 ^{o}C will be tested. Ultimately, the results will be compared to the LEDs with an ImmAg surface finish to determine the impact of surface finish on the strength of these alloys.

(vii) Reliability Study of BGA Assemblies with Mixed Arrays of VIPPO Pads

The PCB via-in-pad plated-over (VIPPO) structure provides design flexibility and space saving in electronics product design. Using VIPPO structures is generally limited to full array of VIPPO pads due to the tendency of mixed arrays to force hot tear like interfacial separations at BGA solder joints during multiple reflows. The separations are caused by tensile stresses imposed by the z-direction differential expansions between select VIPPO sites and their neighboring non VIPPO pad sites. This project will investigate the reliability problems in BGA assemblies with mixed arrays of VIPPO and non VIPPO pads. A test board will be constructed to include microvia-based mixed arrays of VIPPO structures assembled with bare die parts. VIPPO hot tears will be precluded through process means and the effects of mixed microvia arrays on the longevity will be examined through accelerated thermal cycling. The goal to identify particularly risky stacked microvia structures or placement arrangements that should be avoided in product designs.

(viii) Investigation of High Current-Induced Reliability Issues in PCBs

Many of our current stressing studies have focused on the effects of electromigration on solder joints. However, high currents may also have a significant impact on the board reliability. Current flowing through through-holes or slots in multilayer boards can cause localized high temperatures due to joule heating. This overheating issue can be mitigated with additional buried copper layers which help to dissipate heat. Although this method can reduce the temperature below the melting temperature of the SAC solder, there may still be other joint reliability issues arising from high currents and temperatures. This project aims to help develop board design rules avoiding reliability issues in high-current applications.

(ix) Investigating Solder Joint Failure Criterion

Industry standards such as IPC-9701 provide concise definitions for solder joint failure using event detection and/or resistance criteria. However, such standards are somewhat arbitrary and do not necessarily describe when a solder joint is no longer electrically functional for its intended purpose. This project will investigate event detection and resistance criterion and compare the results to solder joint performance in terms of functionality (i.e. data integrity). Our 2025 research portfolio includes an initiative to develop a basic test methodology to perform the comparisons using vibration test protocols to stress solder joints. If successful, the technique may then be applied to other stress conditions such as accelerated thermal cycling and drop testing.

3. Process Development

Successful introduction of a new product requires thorough up-front process development often to levels not anticipated in the new product introduction budget. AREA Principals also have ongoing needs to refine the manufacturing process windows and identify design improvements that can be implemented to improve the yields of existing products with ever-increasing sophistication. With engineering access to state-of-the-art surface mount manufacturing equipment, the AREA Consortium is uniquely suited to develop manufacturing processes for emerging technologies in electronic packaging and assembly. This consortium research thrust will address unique material choices, package designs, component integration, and assembly processes mandated by various integrated electronics of interest to consortium members and their customers.

(i) Solder Void Reduction through Vacuum Reflow

The persistent occurrence of solder voids often diminishes the performance of uniform high conductivity in indium solder interfaces above the die in high power semiconductor packages. Such voids arise during the reflow of fluxed indium solder preforms between silicon die and metal heat spread lids. This project will examine the potential to reduce void formation through the application of vacuum during the indium solder reflow. A simplified sample consisting of a large, metalized silicon die soldered to nickel plated copper heat spreader will be used. Experimental variables of interest include the reflow temperature, vacuum level, and indium bond line thickness. Several In-Ag alloys will be used with Ag content ranging from 0 to 10% Ag. The vacuum reflow experiments will be run in a Heller in-line vacuum reflow oven recently installed in the APL.

(ii) Design and Process Optimization for VIPPO PCB Assemblies

Previous consortium studies have identified the propensity of PCB via-in-pad plated-over (VIPPO) structures to produce interfacial separations at BGA solder joints during second and third reflows. These separations are caused primarily by tensile stresses imposed by the z-direction differential expansions between VIPPO sites and their neighboring pad sites. Methods of precluding these separations are being

examined to determine the proclivity of fault in different process conditions. A test board will be designed with varying counts of vias stacked under BGA pads. These will be placed among differing size via stacks to generate a wide range of differential reflow stresses in the component attachment. The objective is to identify combinations of design and process rules that allow for free usage of VIPPO structures.

(iii) Impact of Edge Bonding and Underfill on Large Body BGA Assembly and Reliability

Large body BGA has become the package of choice for many high-end applications processors, high bandwidth communication devices, gaming systems and graphics. A common BGA package consists of a substrate with several buildup layers on a laminate core, flip-chip attached die, and a metal heat spreader lid attached to the substrate with a perimeter adhesive and in thermal contact with the silicon device through a thermal interface material on the back of the die. For large body BGA packages, the board assembly yield and interconnect reliability are particularly sensitive to the inevitable temperature induced warpage of the package. This project will explore board assembly yield issues for such large body packages and compare the reliability enhancement provided by select encapsulant materials. Large body (≥70 mm) flip-chip BGA packages will be fabricated using thin core (600 µm) laminates, multiple large dummy die and Ni-plated copper lids. The packages will be assembled to appropriately thick circuit boards with conventional SAC305 BGA interconnects. The packages will then be encapsulated with a full capillary underfill and/or edge bonding adhesives using materials selected in consultation with participating member companies. United Adhesives UF1230 and Namics SUF1570-2 are potential candidates underfill candidates. Edge-bonding materials being considered include Panasonic CV5797U and ZYMET UA-3605-B. The BGA assemblies with and without encapsulation will be tested using thermal cycling from -40 to 125 °C, and the solder joint fatigue life of the various assemblies will be compared.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and timely manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Results Reporting

The AREA manager will provide access to key experimental data and the final project reports via the protected consortium website (http://www.apl-uic.com/). Regular consortium meetings will be held in the greater Binghamton area for the purpose of scientific/technical discussion. Presentations made at these meetings will be accessible on-line to Principal companies shortly thereafter. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, and general project status. Principals are encouraged to contact and visit the Advanced Process Laboratory for more effective communication and knowledge transfer. Projects may require the staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.