ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2024 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and electronic assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to engineering topics directly applicable to manufacturing challenges. In every case, the objective is to provide AREA Principals with meaningful results that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a consortium website will be maintained with on-demand content (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals. Longer term reliability evaluation projects may extend into subsequent plan years as needed to complete testing. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities and faculty expertise as needed.

The primary focus for 2024 will be the careful execution of the projects outlined in this document. History indicates that additional topics will be added throughout the year as our capabilities develop, member interests evolve and materials are provided. The research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

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Immersion Gold Surface Finish with Nanoengineered Diffusion Barrier

Electroless Ni-Immersion Au (ENIG) board finishes are often used to improve board assembly soldering yield through improved wettability after extended storage. When used for high frequency applications however the nickel layer at the pad surface leads to an undesirable increased insertion loss at probe sites. Lilotree™ has introduced an alternative, nano-engineered barrier layer between the fusible gold layer and the underlying copper pad. This new surface finish is intended to deliver the soldering benefits of ENIG without the increased insertion loss. This project will evaluate the solderablity of the Lilotree Ni-less finish as well as the joint strength at the soldered interface. The effectiveness of the novel copper diffusion barrier layer will also be explored. Insertion loss will be measured in APL assembled measurement test vehicles.

Thermal Interface Materials

The reliable extraction of excess heat from operating semiconductor devices continues to be a challenge in all sectors of the microelectronics industry. The bulk of consortium thermal interface material (TIM) research to date has focused on second level (metal lid module to aluminum heat sink) interface materials (TIM2). The importance of first level (die to heat spreader) interface material (TIM1) however is well known. Development of experimental capabilities in this space is considered strategic for the consortium research portfolio and steps will be taken to establish this capability in the future.

TIM consortium projects may include material processing and application, nominal thermal performance (conductivity and interfacial resistance) or performance stability in service. Many of the initiatives within

this particular research series may require substantial experimental effort for the design, fabrication and debug of necessary testing apparatus. Some will require iterative enhancement before arriving at final designs and procedures.

Thermal (IR) Imaging for Direct Observation of TIM Stability under Accelerated Power Cycling

The AREA Consortium has developed a test apparatus to monitor the stability of a thermal interface layer directly using IR camera imaging. This technique offers the unique capability of in-situ monitoring of the defect formation and growth in TIMs during power cycling. We will evaluate the performance of this newly developed technique on different types of common thermal interface material i.e., greases and pre-cured gels, phase change material, as well as alternative TIM options such as liquid metal pastes. IR snapshots are continually recorded throughout the test and can clearly show the onset and growth of defects in the TIM layer. High-resolution optical images are also recorded at the end of each test and can be used to confirm the observations made via the IR camera. In addition, the die temperature is monitored in different areas of the die during the test and are useful in correlating the defect formation in TIMs and a local increase in die temperature. An agreement between the IR images, high-resolution optical images and the local die temperature data confirms the applicability of the IR technique for stability analysis of thermal interface compounds. This technique requires the TIMs to be applied between the processing unit (die) and an IR transparent lid (KBr) and will be used for testing commercially available TIM1 and TIM1.5 compounds.

TIM Stability Evaluation under Accelerated Power Cycling

While the IR imaging technique introduced above offers the unique capability of in-situ monitoring of the defect formation and growth in TIMs during accelerated power cycling, the effect of replacing the original copper lid with an IR transparent window is not clear. The KBr window offers a significantly lower thermal conductivity compared to copper. KBr and copper can also have different wettabilities against thermal interface materials that can impact the TIM performance during power cycling. This work intends to determine the applicability of the IR imaging technique for different TIMs by exploring the potential differences in TIM performance when interfaced with a copper lid or a KBr window. To this end, a new thermal test vehicle (TTV) using a CPU package identical to the one used for IR imaging technique (Intel Skylake) is developed. We will use this TTV to evaluate the performance of different types of common thermal interface material i.e., greases and pre-cured gels, phase change material and liquid metal pastes that were already analyzed with the IR technique to identify the differences and similarities. The die temperature is monitored in different areas of the die throughout the test and are useful in correlating the defect formation in TIMs and a local increase in die temperature. High-resolution acoustic images (via C-SAM) are also recorded at specific intervals (every 500 cycles) and can be used to identify any potential degradation in the TIM layer. An agreement between the acoustic images and local die temperature data confirms the applicability of this new analysis technique. Comparison of degradation rate results for identical TIMs can inform on the impact of copper lid replacement in the IR technique.

Thermal Imaging with Laser Flash Analysis with Spatial Resolution

AREA has previously explored the use of selected area laser heating of heat spreader lids to deduce the presence of voids in the underlying TIM layer by analyzing the transient dissipation of heat into the TIM. Spatial resolution of the technique was found to be quite poor. This project will instead use selected area laser heating of an attached heat spreader while monitoring the heat transmitted through the TIM and underlying substrate using and IR imaging camera. The objective will be to quantify the spatial resolution of TIM conduction from the transmitted thermal images.

Stability of Solder Thermal Interface in Accelerated Thermal Cycle

Indium solder thermal interface coupons, comprised of a large silicon die soldered to a plated copper lid, will be vacuum reflowed according to the optimized vacuum reflow profile previously identified for the particular sample configuration of interest. Sample variables will include indium solder composition (0, 3, 10%Ag), solder preform thickness (100, 225, 500um), die size, die thickness, and copper lid thickness. All coupons are expected to have some characteristic defect (void) structure despite the process optimization efforts. Coupons will be thermal cycled (0/100C and -40/125C) and removed at predetermined intervals for x-ray and C-SAM imaging of STIM defect structure. Select samples will further be measured for temperature induced warpage behavior.

Lead-Free Solder Alloy Evaluations

New Pb-free solder alloys with varying alloying elements are being routinely proposed by materials suppliers as replacements (improvements) to the standard SAC305 alloy. Industry interests have been in 1.) low melting temperature solder alloys to minimize the assembly/reliability challenges posed by temperature induced component warpage and 2.) solder alloys with enhanced thermal cycle reliability for harsh environment or mission critical applications.

Projects included in this alternate solder alloy research thrust include evaluations of microstructure and mechanical properties for various solder alloys and surface finishes. The work typically encompasses characterizations for both individual solder balls wetted to a surface finish of interest as well as components assembled onto test boards for second level reliability comparisons through thermal cycle or mechanical testing. The performance of the alternative lead free alloy solder joints is often compared to that of the common SAC305 alloy or eutectic SnPb, as appropriate.

Reliability of SAC305 Mixed Assembly Joints formed with High Reliability Solder Pastes

Many so-called High Reliability solder alloys, based on modifications to the ubiquitous SAC305 formulation, have been introduced with the promise of improved thermal cycle reliability. Most such alloys include solid solution levels of Bi. For the most part, these alloys have not yet been adopted by the

semiconductor packaging industry. BGA components are therefore not yet available with solder balls of these various high reliability alloys. Early adopters of such high reliability solder pastes are therefore forced to mix the paste alloy with the SAC305 sphere in card assembly. Since SAC305 spheres will melt during the reflow of hi-rel solder paste, the solder joint mixing will be more complete than in previous mixing cases in which only the paste melted but the strengthening effects of the Bi will be dramatically diluted, thereby reducing its reliability benefit. High reliability solder pastes of interest include Cyclomax (SAC-Q), MaxRel, Alpha C10, Senju M58 and Indium Duafuse HR. The reliability of these mixed alloy solder joints will be tested with -40 to 125C cycle in a variety of common BGA package types. Paste printing and reflow process optimization trials will be run for all alloy prior to building the final test assemblies.

Solder Joint Shear Strength of Select High Reliability Solder Alloys

The reliability of solder alloys in cyclic stress applications is often seen to scale with strength; higher strength alloys are better able to withstand the stresses imposed by cyclic thermal expansion mismatch or the mechanical loading in vibratory applications. Our latest crop of high reliability alloys will therefore be screened with solder joint shear testing before proceeding with other reliability tesitng. 0.4mm spheres will be soldered to 0.38mm SMD pad and shear loaded at fixed displacement rates. Loads to failure will be measured at temperatures from 20C to 80C. Alloys to be screened will include iSenju M58, Cyclomax (SAC-Q), Alpha C10, and Durafuse HR. This test will be used to downselect the alloys to be used in subsequent vibration reliability testing.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

Double Reflow BGA Soldering Defects over Stacked Microvias

Previous consortium studies have identified the propensity of PCB via-in-pad, plated-over (VIPPO) structures to produce interfacial separations at BGA solder joints during second and third reflows. These separations are caused by tensile stresses imposed by the z-direction differential expansions between

select VIPPO sites and their neighboring pad sites. This project will similarly examine BGA assemblies over various stacked microvia structures for such solder joint defects when subjected to multiple reflows. A test board will be designed with varying counts of vias stacked under BGA pads. These will be placed among differing size via stacks to generate a wide range of differential reflow stresses in the component attachment. The objective will be to identify particularly risky stacked microvia structures or placement arrangements that should be avoided in product designs.

Effect of Solder Joint Volume on Drop Shock Performance by Solder Alloy

Recent consortium comparisons of drop shock performance of several different solder alloys revealed an apparent dependence of the alloy performance ranking on solder joint volume. (Here, joint volume refers to solder joint dimensions, or perhaps simply solder joint height.) The relative drop life performance of SAC305 and SnPb eutectic solder joints can be reversed for different solder volume joints on same package footprint (LGA vs BGA, for instance) presumably indicating that the solder joint mechanical response of a given solder alloy depends on the stress state being imposed. This project will study the solder volume effects on drop shock lifetime in a more systematic way, examining solder alloy ranking with progressively larger solder joints. A 196 I/O full array package will be assembled with a range of solder joint sizes (LGA through full BGA) for systematic drop shock testing. Finite element analysis will be included as needed to understand the stress state variation with solder joint volume.

Interfacial Bismuth Accumulation Impact on Solder Joint Drop Shock Response

Under electromigration (DC current) stresses, low temperature BiSn solder joints are known to accumulate continuous layers of bismuth at the anodic interface of the joint. This layer can have a measurable effect on the resistance of the solder but will not necessarily create an electrical failure in the test circuit. For some applications (laptops, tablets, etc.) of greater concern will be the possibility of increased solder joint fragility introduces by the brittle bismuth layer at the interface. Knowing the rate of bismuth accumulation as a function of current density and temperature, BGA solder joints in the AREA BGA196 drop test board will be modified through the application of current to have predictable layers of bismuth phase on pre-determined solder joint interfaces (component or board side). Test boards will then be subjected to repetitive drop shock loadings to failure. Results are to be compared to that of corresponding solder joints in the as-reflowed state to quantify any increased joint fragility. Time after reflow has also been found to be key variable in LTS drop shock performance and thus will be monitored for all drop samples.

Effect of Electromigration Pre-Stress on Thermal Cycle Lifetime of LTS Joints

Previous efforts to evaluate the reliability impact of current stress on the thermal cycle lifetime of low temperature solder BGA joints was fraught with experimental difficulties. Only a limited number of test nets could be wired for direct current flow during the thermal cycle. Excessive joule heating of the sample would result if all test nets were exposed to current. All BGA solder joints are however stressed during

the environmental thermal cycle of an attached processor module. Attempts to select which nets would fail in thermal cycle such that those could be simultaneously current stressed proved unsuccessful. In this follow-on project, all test nets will be uniformly pre-stress with electric current. Samples thus pre-stressed will then thermal cycled without superimposed current flow. This way any joint that fails in thermal cycle would have first experienced a known level of electric current stress.

Drop Shock Reliability of Cyclomax Solder Joints

Cyclomax is SAC based solder alloy with 3.3%Bi. Such low-level additions of Bi have been shown to improve thermal cycle reliability but their effect on drop shock performance is unknown. At higher concentrations, Bi generally degrades the drop shock performance significantly. This experiment will evaluate drop shock life of BGA208 components assembled with homogenous Cyclomax BGA joints and compare results to otherwise equivalent SAC305 assemblies. Multiple reflows, up to 5X, will performed on select samples prior to dropping.

FEM Investigation of Solder Joint Residual Stress as a Function of Solidification Temperature

AREA Consortium accelerated thermal cycle testing has convincingly demonstrated that the thermal cycle reliability of homogenous low temperature (SnBi) BGA joints exceed that of homogeneous SnAgCu BGA joints. This result could be simply ascribed to superior fatigue resistance of the near eutectic SnBi alloy relative to the ternary SnAgCu alloys. That however would be counterintuitive, given the higher homologous temperature cyclic stresses in the low temperature solder case. An alternate hypothesis would be to ascribe the effect to the differing tensile stresses imposed on the BGA joints from temperature induced component warpage. The residual stress imposed on the BGA joints from a warping component is determined solely by the solidification temperature of the solder. A higher solidification temperature, as would be experienced with SnAgCu solder, imposes a much greater room temperature residual stress on the solder joint. This higher stress will be experienced throughout the thermal cycle. Since it is not possible to experimentally change the solder alloy (and thus properties) independent of the solidification temperature, this hytpothesis will be explored through numerical simulations—changing the solidification temperature and thus residual stress while keeping the alloy constant. SnPb thermal cycles will be simulated with zero stress states defined at different solidification temperatures.

Vibration Fatigue Response of High Reliability Solder Alloys

The vibration lifetime of two high reliability solder alloys will be tested using APL fabricated BGA test components. Two solder alloys from those alloys available to us as sphere preforms will be selected based on solder joint shear strength testing. 1mm BGA556 test components will be balled in the APL with the solder alloy spheres of interest and then attached to the vibration test board using the corresponding alloy paste. Subsequent testing will thus be done on assembled test cards with homogenous alloy joints. Vibration testing will be done with sinusoidal loading imposed at the resonant frequency determined for

the board. BGA test nets will be monitored for electrical failure. Elevated temperature vibration tests will be run at 80C and comparted to results from room temperature vibration runs. Homogeneous SAC305 and SnPb solder joints will also be tested for reference.

Assembly Process Development

With engineering access to state of the art surface mount manufacturing equipment, the AREA Consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy member access in addition to the final project reports (http://www.uic-apl.com/databases).

Solder Thermal Interface Vacuum Reflow Assembly

The persistent occurrence of solder voids often diminishes the performance of uniform high conductivity in indium solder interfaces above the die in high power semiconductor packages. Such voids arise during the reflow of fluxed indium solder preforms between silicon die and metal heat spread lids. This project will examine the potential to reduce void formation through the application of vacuum during the indium solder reflow. A simplified sample consisting of a large, metalized silicon die soldered to nickel plated copper heat spreader will be used. Experimental variables of interest include reflow temperature, vacuum level, and indium bond line thickness. Several In-Ag alloys will be used with Ag content ranging from 0 to 10% Ag. Vacuum reflow experiments will be run on a Heller in-line vacuum reflow oven now installed in the APL.

Selected Area Laser Reflow Thermal Limitations

The promise of controlled local solder reflow using a laser with selected area optics can often be confounded by the differing thermal response of various board and component materials to the impinging laser light. This project explores the limitations of a selected area laser to produce uniform temperature solder reflow using a range of board structures (varying copper content), component types and the APL selected area laser reflow tool.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and useful manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Projects may require the staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.