ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2021 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and electronic assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to engineering topics directly applicable to manufacturing challenges. In every case, the objective is to provide AREA Principals with meaningful results that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a consortium website will be maintained with on-demand content (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals. Longer term reliability evaluation projects may extend into subsequent plan years as needed to complete testing. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities and faculty expertise as needed.

The primary focus for 2021 will be the careful execution of the projects outlined in this document. History indicates that additional topics will be added throughout the year as our capabilities develop, member interests evolve and materials are provided. The research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

MAT1C. Edge Bonding of BGA Components

The use of encapsulation to improve the reliability of component to board interconnects requires not only selection of the appropriate material but also specification of the extent of underfill required. Edge bonding may well be adequate for the mechanical robustness required and even superior to full capillary underfill for thermal cycle reliability. Other benefits of partial encapsulation schemes may include reduced process time and materials consumption. Enhanced reworkability is a further cited advantage of partial underfill over full capillary underfill encapsulation given the easier component removal and site dress. This study compares the effectiveness of reliability enhancement provided by several encapsulant materials applied to six different area array packages with package body sizes ranging from 12mm square to 31mm square. Reliability performance will be monitored using the (-40 to 125C) cycling profile; no other mechanical or shock load tests are included. Two capillary underfill materials (United Adhesives UF1230 and Namics SUF1570-2) and three edge-bonding materials (Panasonic CV5797U, ZYMET UA-3307-B and ZYMET UA-3605-B) are being evaluated. Project progress to date includes assembly and reliability test of capillary underfill and no underfill control samples. Edge bonding cells include evaluation of material dispensing attributes, comparing for instance various available dispensing technologies (e.g., auger pump vs. jetting). 2021 will include assembly and test of the final edge bond material (Panasonic).

MAT2D. Pad Cratering Behavior of Laminate Cap Layers under Imposed Bending Strains

Member companies with mission critical PCBA products continue to be plagued by pad cratering of PCB laminate materials due to induced board strains under critical large components. Several member companies had previously developed robust product (that is, resistant to laminate pad cratering) using the reinforcement of the laminate surface with a tough cap layer. ZetaCap is a popular example of such a cap layer laminate. ZetaCap has recently been declared end of life by its supplier so viable replacements are of interest. This project, started in 2020, explicitly compares several cap layer options that may serve as replacement materials for ZetaCap applications. It uses a previously defined consortium test method

for comparing pad cratering tendencies among different laminate materials using a cyclic four point bend test. In this vehicle two BGA components are assembled along the axis of board bend in order to impose tensile strains along the outer BGA solder joints which promote laminate pad cratering especially under the corner solder joints. Test traces emanate from the corner joints to allow electrical monitoring of the completed cratering event. 2021 tasks will include the completion of all monotonic bend test cells as well as evaluate the possible inclusion of harmonic vibration test cells using the same single axis bend test boards. The test board has been designed to also accommodate a similar pad cratering comparison through harmonic vibration. Such vibration testing is anticipated as a follow-on activity likely extending into 2022.

MAT4 Series: Thermal Interface Materials

The reliable extraction of excess heat from operating semiconductor devices continues to be a challenge in all sectors of the microelectronics industry. The bulk of consortium thermal interface material (TIM) research to date has focused on second level (metal lid module to aluminum heat sink) interface materials (TIM2). The importance of first level (die to heat spreader) interface material (TIM1) however is well recognized. Development of experimental capabilities in this space is considered strategic for the consortium research portfolio and steps will be taken to establish this capability in the future.

TIM consortium projects may include material processing and application, nominal thermal performance (conductivity and interfacial resistance) or performance stability in service. Many of the initiatives within this particular research series may require substantial experimental effort for the design, fabrication and debug of necessary testing apparatus. Some will require iterative enhancement before arriving at final designs and procedures.

MAT4B. Graphite Thermal Pad Reliability and Monitor Apparatus

The reliability of a select subset of candidate graphite pad thermal interface materials (e.g., Jones 21-1500, Allied SO1500, Nolato 9610 and Nolato 9450 pads) is being compared through 0-100C accelerated thermal cycling of a test structure having multiple graphite pads bonded to a common aluminum heatsink structure. Graphite based thermal pads are electrically conductive and thus not suited for the capacitance based reliability test method previously used for other TIM2 materials. An alternative method of monitoring electrical resistance across the interface is being actively developed in this project. Post-test construction analysis will be performed at all pad sites to evaluate physical bond integrity and correlate observed physical phenomena with recorded electrical resistance response. The goal of this project would be to establish a reliability test method and apparatus applicable to electrically conductive TIMs.

MAT4D. Thermal Cycle Instability in Gallium-Indium Liquid Metal Thermal Interfaces

Gallium Indium eutectic liquid provides a highly effective thermal interface for high power devices, providing both high thermal conductivity and the inherent dimensional compliance of a low viscosity

liquid. Apart from assembly processing challenges, the operational stability of such a system can be suspect for many applications. Thermal cycling, especially with low temperature excursions, is known to degrade the thermal conductivity of such liquid Ga-In interfaces. The mechanism of thermal degradation is as yet uncertain. This study is a continuation of the 2020 introductory exploration of Ga-In TIMs. It will investigate the thermal cycle stability of Ga-In and GaInSn alloys using repetitive differential scanning calorimetry exposures. The objective will be to replicate the low temperature degradation phenomenon, identify the mechanism, and enable potential remedies.

MAT4E. Interval Testing of TIMs in Thermal Cycle: Test Apparatus Development

Using in-situ electrical capacitance monitoring of dielectric thermal interface materials has been shown to be a viable experimental method of monitoring the physical degradation of second level thermal interfaces in accelerated thermal cycle. The exact correlation of such physical degradation to thermal conductivity performance however is largely unknown. This project will build and test a first generation apparatus that allows for interrupting such monitored thermal cycle testing of TIM structures and installing a power device to enable direct steady state heat flow performance through the TIM stack at select cycling intervals.

MAT7 Series: Lead-Free Solder Alloy Evaluations

New Pb-free solder alloys with varying alloying elements are being routinely proposed by materials suppliers as replacements (improvements) to the standard SAC305 alloy. Industry interests have been in 1.) low melting temperature solder alloys to minimize the assembly/reliability challenges posed by temperature induced component warpage and 2.) solder alloys with enhanced thermal cycle reliability for harsh environment or mission critical applications.

Projects included in this alternate solder alloy research thrust include evaluations of microstructure and mechanical properties for various solder alloys and surface finishes. The work typically encompasses characterizations for both individual solder balls wetted to a surface finish of interest as well as components assembled onto test boards for second level reliability comparisons through thermal cycle or mechanical testing. The performance of the alternative lead free alloy solder joints is often compared to that of the common SAC305 alloy or eutectic SnPb, as appropriate.

MAT7A. High Reliability Pb-free Solder Alloys: Thermal Cycle Profile Effects

Product implementation of recently proposed high reliability Pb-free solder alloys has been impeded by a lack of experimental data informing the extraploation of laboratory thermal cycle reliabily results to field conditions with extended thermal cycle dwell times. While the AREA Consortium has actively evaluated the thermal cycle reliability of many of these commercially proposed alternative Pb-free solder alloys these comparisons have been done often using a single thermal cycle profile. No basis exists with which to extrapolate these results to field conditions. 2020 research compared the mechanical behavior of

select high reliability alloys under conditions of various elevated temperature dwell times including correlation with microstructural observations. The next iteration in this thrust will be a comparison of thermal cycle and thermal shock performance, specifically focused on the third generation of Pb-free alloys (Bi strengthening along with several other alloying elements). This experiment will include the effect of package stiffness through the comparison of fatigue performance on aluminum T-Clad substrates to that with conventional laminate substrates.

MAT7H. Thermal Cycle Reliability of Low Temperature Solder BGA Joints

Thermal cycle reliability testing of homogenous BiSn(Ag) solder joints (*i.e.*, BiSn(Ag) spheres on BiSn(Ag) paste) was initiated in 2019; cyclic testing will continue through 2021. This reliability test uses an AREA designed test board that includes BGA228, BGA208, BGA196 and one stitched RLDRAM memory component all balled with BiSn eutectic 1%Ag solder alloy spheres. All BGAs were attached with the same composition paste, either BiSn1Ag or the Nihon Superior LT1 off-eutectic (low Bi) alloy. BGA pitches on test include 0.5 mm, 0.8 mm, and 1.0 mm. Thermal cycling with profiles 0/100C and -40/105C through 2020 has failed much of the larger body componentry. Cycling will continue to generate failures in longer lived components such as the MLF72 and SMR passives.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

REL8A. Wafer Level Chip Scale Package (WLCSP) Interconnect Reliability without Post Chip Join Cleaning

In a 2019 consortium study, WLCSP devices with 0.30mm thick die were found to be quite robust in thermal cycle when appropriately underfilled. According to best practices, the prior test parts were cleaned prior to device underfill to promote encapsulation integrity. Given the acceptable reliability of these parts in the underfilled state, a 2020 follow-up study was initiated to investigate the elimination of post chip join wash prior to underfill as a manufacturing cost savings. This follow-up project is exploring the thermal cycle reliability limits of larger body WLCSPs (up to 12 mm) using electrically stitched devices

in a -40/125C thermal cycle. The previously used WLCSP body sizes (4, 5, 6, 8, 10, 12 mm square) are also being tested using the same test board laminate materials (including Elite EM526). WLCSP assembly included both flux dip and paste dip chip joining processes. All devices were underfilled with Loctite 8803S. Thermal cycle reliability of this test population has proven to be reasonably robust; thermal cycling and failure analysis will continue into 2021.

REL9A. Mixed VIPPO (Via-In-Pad, Plated Over) Array Induced BGA Solder Defects

Solder joint interfacial separation at BGA joints above Via-in-Pad Plated-Over (VIPPO) connected solder pads during second reflow events is a persistent problem for lead free BGA components on complex board assemblies. Experimental investigation of this phenomenon has been underway in the consortium research portfolio for several years using a custom test board design. This test board emulates the behavior of relatively thick boards (>110 mil) for complex network/server applications. It includes BGA footprints with varying VIPPO/non-VIPPO densities and intermixing configurations with and without backdrilling. Experimentation using this particular test board is complete. Key observations have been made with this vehicle regarding VIPPO design attributes as well as solder reflow environment, flux coverage, and solder alloy selection. Two different 1.0 mm pitch lidded BGA parts showed minimal propensity for VIPPO solder defects while the two standard BGA memory packages were much more prone to VIPPO defects depending on the exact reflow conditions imposed. The 2021 research plan will pursue another iteration of the VIPPO experimental exploration. Some additional optical metrology methods will be attempted to characterize the temperature induced topography of BGA pad footprints in the vicinity of VIPPO pads. A second iteration of the VIPPO test board will be designed and fabricated for the investigation of laminate material and board thickness effects.

REL10C. Effect of Solder Joint Volume on Drop Shock Performance by Solder Alloy

Recent consortium comparisons of drop shock performance of several different solder alloys revealed an apparent dependence of the alloy performance ranking on solder joint volume. (Here, joint volume predominately refers to solder joint size, or perhaps simply solder joint height.) The relative drop life performance of SAC305 and SnPb eutectic solder joints can be reversed for different solder volume joints on same package footprint (LGA vs BGA, for instance) presumably indicating that the solder joint mechanical response of a given solder alloy depends on the stress state being imposed. This project will study the solder volume effects on drop shock lifetime in a more systematic way, examining solder alloy ranking with progressively larger solder joints. A 196 I/O full array package will be assembled with a range of solder joint sizes (LGA through full BGA) for systematic drop shock testing. Finite element analysis will be included as needed to understand the stress state variation with solder joint volume.

REL10D. Interfacial Bismuth Accumulation Impact on Solder Joint Drop Shock Response

Under electromigration stresses, low temperature BiSn solder joints are known to accumulate continuous layers of bismuth at the anodic interface of the joint. This layer can have a measurable effect on the

resistance of the solder but will not necessarily create an electrical failure in the test circuit. For some applications (laptops, tablets, etc.) of greater concern will be the possibility of increased solder joint fragility introduces by the brittle bismuth layer at the interface. Knowing the rate of bismuth accumulation as a function of current density and temperature, BGA solder joints in the AREA BGA196 drop test board will be modified through the application of current to have predictable layers of bismuth phase on pre-determined solder joint interfaces (component or board side). Test boards will then be subjected to repetitive drop shock loadings to failure. Results are to be compared to that of corresponding solder joints in the as-reflowed state to quantify any increased joint fragility.

REL15B. Power Cycle Reliability of QFN Packages

Wirebond QFN packages containing resistive test die were fabricated using open body 0.4 mm pitch QFN packages (12.0 x 10.5 mm) gloptopped with a filled epoxy encapsulant to create testable packages that are structurally representative of epoxy overmolded QFNs. In 2019, these custom QFNs were placed on power cycle test using a 10 minute square wave of DC current (0.5A) that heats the package to 125C in the current ON condition. These packages, with improved thermal path over the previously tested snap top packages, are proving far more robust in power cycle. 17000 power cycles had accumulated at year end 2020 with no failures. Power cycling will continue through 2021 attempting to generate solder interconnect failures.

REL16B. Reliability Impact of Leadless Solder Joint Castellations

SMT solder joints for leadless packages such as QFNs are typically designed such that the PCB mounting pad extends beyond the package body. The resulting solder joints therefore include a fillet extending up the side of the package and outward away from the package body. These protruding solder fillets are generally perceived to be advantageous from a thermal cycle reliability standpoint. On the other hand, removing this castellation from joint design reduces the board footprint and enables higher density placement of such leadless packages on the circuit board. The magnitude of the reliability enhancement of the joint castellation is unknown. This project will experimentally quantify the reliability impact of such solder joint castellations. At a minimum, SnPb and SAC305 solder compositions will be used. Half-length fillets and a zero length fillets will be designed into a QFN reliability test board using the standard fillet length case as a baseline control. Assembled boards will be testing in thermal cycle with in-situ event detection. For any given pad design, solder volume is expected to have a measureable impact on thermal cycle reliability and will thus be another potential experimental variable.

REL17B. Electromigration Behavior in Near Eutectic BiSn Solder Alloys

Industry interest in the possiblity of lower temperature reflow soldering continues unabated. One key attribute of various low temperature alloys that remains to be vetted is the microstructural stability under extended electric current flow. Previous AREA research has demonstrated that Bi phases in near-eutectic BiSn alloys migrates considerably and predictably under the influence of constant electric current at high homologous temperatures. The solder supplier community has embrace industry interest in low

temperature soldering by offering an array of different BiSn alloys with different elemental additions.

characterize the redistribution of bismuth phases in the solder joint microstructures of near eutectic BiSn solder alloys. The effect of these secondary alloying elements on electromigration kinectics is largely unknown. 2021 research will include direct comparisons of Bi migration under constant current stress in near-eutectic alloy offerings by Senju (L29), Eunow (DW-1000) and Shenmao (PF-735).

REL17D. Thermal Cycle Reliability of LTS Solder Joints under Electric Current Stress

Low temperature solder (LTS) joints containing bismuth are prone to dramatic microstructural changes when exposed to extended electric current stress at elevated temperatures. Mobile Bi atoms subjected to an electron wind accumulate at the anode side of a solder joint. This microstructural change and associated modification of mechanical behavior may well impact the ability of such joints to tolerate the accumulating cyclic strains imposed by an environmental thermal cycle. This study will subject stitched BGA nets in a board attached, large die laminate BGA package to a steady current flow while thermal cycling in an environmental chamber. Moderate current densities will be used to minimize local joule heating of the package. The ambient thermal cycle will nonetheless be adjusted to accommodate the measured joule heating and thereby control the peak cyclic temperatures experienced by the solder joints. In-situ event detection will be used to capture joint failures. Metallographic cross-sectioning will be used to identify the microstructural fatigue mechanisms operative under persistent current flow being mindful of the direction of electron flow in the particular failing joint of interest.

REL17E. Model for Bismuth Electromigration in Low Temperature BiSn Solder Joints

Prior AREA research has used mixed BiSn-SAC305 solder joints to experimentally determine the combined electromigration parameter DZ* (diffusivity $\times$ effective charge number) for bismuth in a tin matrix. This parameter is critical for describing the migration of Bi as a function of current density and temperature in BiSn based low temperature solder joints. Using a the recently designed AREA electromigration test coupon to provide quantitative joint resistivity measurements, this project will develop a model for Mean Time to Failure (MTTF) according to common failure criteria (a JEDEC recommended 20% solder joint resistance increase, for instance). The model will express MTTF as function of the critical product design parameters temperature, current density and solder joint height as well as the solder alloy bismuth content.

REL19A. Thermal Stability of Electrolytic Capacitors

The materials and construction of electrolytic capacitors are well known to be susceptible to temperature induced degradation. High peak soldering temperatures along with extended times at elevated operating temperatures can produce substantial degradation in electrical performance. Degradation can take the form of decreased capacitance over time or more often increased equivalent series resistance. This

project will monitor the equivalent series resistance and capacitance of nine different electrolytic capacitor part numbers as a function of thermal exposure. Assembly process will include solder reflows at 245C (2X) or 260C (2X, 3X). Assembled capacitors will be tested after various intervals of elevated temperature storage. Capacitor types will include cylindrical can and solid polymer body types.

REL19B. Strain Induced Cracking of Multilayer Ceramic Capacitors

Printed circuit board assemblies, particularly those intended for server applications, are often affixed to rigid metal frames with screws passing through tooling holes in the board. The associated mounting stresses impose local board bending strains around these tooling holes. Such bending strains are known to induce internal cracking in the body of multilayer ceramic capacitors mounted in the vicinity of the tooling holes, producing electrical functionality anomalies. These capacitor defects are introduced during server level assembly, after SMT final card test, and thus escape detection in the manufacturing process. The limiting board bending strain required to produce MLCC cracking during box assembly has not been rigorously documented. This project will explore those limits for various MLCC part number imposed to increasing levels of board bending strain at different strain rates. Four different capacitor formats (0603, 0805, 1206, 1210) will be evaluated.

Assembly Process Development

With engineering access to state of the art surface mount manufacturing equipment, the AREA Consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy member access in addition to the final project reports (http://www.uic-apl.com/databases).

APD1D. Solder Dispensed Repair of Low Volume Print Deposits

Previous consortium research explored the reliability consequences of low volume solder paste print deposits on both BGA and BTC components. Intentionally created low volume deposits with reduced stencil apertures at key risk sites was able to demonstrate both negative and positive effects of paste print

defects. Low volume deposits were the most detrimental for Bottom Terminated Components such as LGA parts, producing measurable reductions in thermal cycle reliability. To mitigate this problem, Koh Young is now offering solder paste inspection tools with an on-board solder paste dispenser to replenish low volume deposits as they are detected. A Koh Young 8030-3 SPI tool with such a solder jet dispense head has been installed in the APL for evaluation trials. Using a previously designed test board/stencil combinations to produce controlled print defects, individually dispensed print reworks will be selectively programmed for product quality and reliability evaluation. A standard SAC305 solder paste will be used

APD 4C. Rework of Underfilled BGA Components using Milling Removal

Periodic rework of BGA components (*i.e.,* removal and replacement) is a necessity for most surface mount assembly manufacturing lines. The process for removing soldered components, site dressing and re-soldering is fairly well established and dedicated tools for this purpose are readily available. The need for added interconnect robustness in many applications has increased the practice of underfilling components after solder attach with filled epoxy materials. BGA component rework after such underfill encapsulation becomes significantly more challenging. When solder joints are fully encapsulated simply melting the solder joints does not release the part from the board. AirVac, a well-known provider of rework manufacturing tools, has recently been promoting the practice of machining off defective components from a board if they are fully underfilled. This capability is offered as a built-in tool option in their AVX-250 rework system. AirVac was unable to provide such a tool to the APL in 2020 pending final tool definition. It has however committed to do so in midyear 2021, at which time, we will explore the process of milled component rework, establishing for instance how close to the board surface must the underfill be milled to get a reliable reconnection. Similarly, the robustness of the processes for site dress and resoldering of new BGA components to milled encapsulant surfaces will be explored.

APD 4D. BGA Pad Repair using Aerosol Jet Printing

Removal and replacement of defective BGA components is an inevitable requirement of any surface mount assembly manufacturing operation. Local hot air reflow and removal of such components can be difficult for thermally massive large body packages. Cooler temperatures at corner solder joints can result in fully intact solder joints at the corners during physical removal of the part. Solder pads can thus be ripped from the board. This project will explore the use of aerosol jet printing of copper based conductive inks to replace the missing pad. Jetting processes will be developed to replicate a viable pad structure connected to the remaining fractured trace or microvia. Reattachment of BGA solder joints to these repair structures will be demonstrated. Evaluations will include some preliminary testing to assess the viability of such repair interterconnects.

APD11A. Application Process for Gallium-Indium Liquid Metal Thermal Interfaces

Gallium Indium eutectic liquid provides a highly effective thermal interface for high power devices. The high thermal conductivity and dimensional compliance offered by a liquid interface is particularly desirable for die level (TIM1) thermal solutions. Ga-In liquid wets a wide range of surfaces but often requires mechanical manipulation of the liquid against the surface of interest and produces variable results. Such operator-dependent, manual manipulation is not conducive to large scale manufacturing. This project explores options for automated processing of gallium-indium based liquid metals in thermal interface applications. These efforts will primarily be based on published observations that inert particulate loading of liquid metals affects their wetting and spreading characteristics. Experiments will include processing of GaIn and GaInSn liquids with inert Ni, W, and stainless steel particles as well as reactive Cu powder. Characterization of the effects on wetting and spreading on silicon or nickel plated surfaces will include stencil printing trials as may be required for manufacturing application of TIM1.

Advanced Semiconductor Packaging

A new consortium research thrust was proposed in 2020 to address unique package designs and assembly processes envisioned for heterogeneous package structures of interest to consortium members and their product development teams. AREA recognizes the active interest in heterogeneously integrated packaging technologies among several Consortium Principals motivating the Heterogeneous Packaging Integration project proposed in the 2020 Research Plan. Industry wide disruptions in the global supply chain for semiconductor devices in 2020 has precluded the sourcing of necessary test die for project execution. This lack of test die (or chiplets) is expected to continue through 2021. As such, no commitment for a semiconductor device packaging project (heterogeneous or otherwise) will be documented in the 2021. Efforts will however be made throughout the year to identify willing sources of test devices for meaningful evaluations within the consortium. A research project appropriate for any such available devices thus identified will be proposed and reviewed with interested Principals for revision and incorporation into the AREA research portfolio.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and useful manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Projects may require the staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.