ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2020 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and electronic assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to engineering topics directly applicable to manufacturing challenges. In every case, the objective is to provide AREA Principals with meaningful results that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a consortium website will be maintained with on-demand content (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals. Longer term reliability evaluation projects may extend into subsequent plan years as needed to complete testing. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities and faculty expertise as needed.

The primary focus for 2019 will be the careful execution of the projects outlined in this document. History indicates that additional topics will be added throughout the year as our capabilities develop, member interests evolve and materials are provided. The research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

MAT1C. Edge Bonding of BGA Components

The use of encapsulation to improve the reliability of component to board interconnects requires not only selection of the appropriate material but also specification of the extent of underfill required. In many cases, edge bonding and corner bonding may well be adequate for the mechanical robustness required and even superior to full capillary underfill for thermal cycle reliability. Other anticipated benefits of partial encapsulation schemes include reduced process time and materials consumption. Enhanced reworkability is a further cited advantage over full underfill encapsulation given the easier component removal and site dress with partial underfill configurations. This study will compare the effectiveness of the reliability enhancement provided by several recent material offerings applied to six different area array packages with package body sizes ranging from 12mm square to 31mm square. Two capillary underfill materials (United Adhesives UF1230 and Namics SUF1570-2) and three edge-bonding materials (Namics SUF1583-19, ZYMET UA-3307-B and ZYMET UA-3605-B) are being evaluated. UA-2605 is identified as reworkable material. This study already in progress is focusing solely on encapsulation process and thermal cycle reliability performance (-40 to 125C); no other mechanical or shock loadings are being imposed. Project progress to date includes assembly of capillary underfill and no underfill control samples and a start on thermal cycle reliability testing. Edge bonding efforts have been focused exclusively on material dispensing attributes comparing for instance various available dispensing technologies (e.g., auger pump vs. jetting). Care has been taken to characterize the intrusion of encapsulant material into the component solder ball array. 2020 will complete encapsulation process definition for remaining materials, encapsulation bonding of all remaining reliability test cells and completion of the thermal cycle stress testing. Detailed failure analyses will of course follow.

MAT2D. Pad Cratering Behavior in Cyclic Bend Test by Laminate Material

Several member companies continue to be plagued by pad cratering of laminate materials under critical large components during assembly induced board strains. This project revisits a previously defined

consortium test method for comparing pad cratering tendencies among different laminate materials using a cyclic four point bend test. In this vehicle two BGA components are assembled along the axis of board bend in order to impose tensile strains along the outer BGA solder joints which promote laminate pad cratering especially under the corner solder joints. Test traces emanate from the corner joints to allow electrical monitoring of the completed cratering event. In the present study, the pad cratering tendency of several high performance laminates such as Megtron 6 and Nelco 4800 will be compared to our commonly used 370HR laminate material.

MAT4B. Graphite Thermal Pad Reliability

The reliability of a select subset of the candidate graphite pad thermal interface materials (e.g., Jones 21-1500, Allied SO1500, Nolato 9610 and Nolato 9450 pads) will compared using accelerated thermal cycling of a multiple pad – common heatsink structure. These graphite based pad materials are electrically conductive and thus not suited for the capacitance based reliability test method previously used for other TIM2 materials. An alternative method of monitoring electrical resistance across the interface will be investigated. Post-test construction analysis will be performed at sites to evaluate physical bond integrity at test termination.

MAT4C. Reliability of Thermal Greases for Heatsink Applications

The performance of thermal interface materials for heat sink applications is typically reported as bulk thermal conductivity measured in the as-applied state. The stability of this condition may however be suspect with thermal performance degrading with system operating hours. This on-going project monitors the stability of TIM2 materials using a capacitance measurement across the TIM bondline. A custom test apparatus mimics the TIM bond to an aluminum heatsink. The prepared thermal interface is stressed in an environmental thermal cycle at individual sites having a range of different distances from the system neutral point of a common aluminum heatspreader. Thermal expansion mismatch with the mated circuit board imposes a cyclic shear load on the TIM2 bondlines that may degrade the TIM thermal performance. Using the mathematical analog between capacitance and thermal conductance, the degradation of TIM performance is measured independently at each test site. An additional capacitive test apparatus designed specifically to accommodate thin thermal grease bondlines (0.1μm) was fabricated in 2019. This will be used in 2020 to evaluate the following thermal grease materials: Laird T-Grease 2500, Nolato 9540 Grease and Jones 21-430SF Grease.

MAT4D. Gallium-Indium Liquid Metal Thermal Interfaces

Gallium Indium eutectic liquid provides a highly effective thermal interface for high power devices. The high thermal conductivity and dimensional compliance offered by liquid interface is highly desirable. The stability of such a system however poses engineering challenges. This introductory study will focus on processing characteristics to apply the material with adequate wetting and also to investigate the thermal cycle stability of the thermal interface system. Thermal cycling, especially with low temperature

excursions, is known to degrade the thermal conductivity of Ga-In interfaces. The mechanism of thermal degradation is as yet uncertain. Experimental attempts are planned to replicate this degradation phenomenon and identify the mechanism to enable potential remedies.

MAT6 Series: Harsh Environment Electronic Interconnect

As electronics become integrated into higher temperature environments such as those associated with electronic engine controls in the automotive and aviation applications, higher melting temperature and more thermally stable solder alternatives are being explored. Our harsh environment electronics thrust continues to probe solder alloys intended for both die level and board level metallic interconnects in high reliability high temperature electronics applications.

MAT6C. Semi-Sintering Silver Die Attach Materials

New silver filled adhesive materials have been introduced to the market that purport to offer the lower processing temperature advantages of silver filled epoxies and the high thermal conductivity of fully sintering silver pastes. This project will be a first look at these so-called semi-sintering paste materials. Rather than forming a conductive path along a percolation path of mechanically contacting Ag flakes, these semi-sintering materials enable the sintering of contacting silver particles into a solid metal path during the cure cycle. The project will examine the processing characteristics of these materials, in particular stencil printing behavior. Using nominal cure schedules, the bonding characteristics to copper T-Clad substrates and silicon die as might be used in high power device applications will be investigated. Simple device shear testing and detailed microstructural characterization will be the primary experimental approach. Initial experiments will use Ablestik ABP 8068T.

MAT7 Series: Lead-Free Solder Alloy Evaluations

New lead free solder alloys with various alternative alloying elements are being routinely proposed by materials suppliers as replacements (improvements) to the standard SAC305 alloy. Industry interests have been in 1.) low melting temperature solder alloys to minimize the assembly/reliability challenges posed by temperature induced component warpage and 2.) solder alloys with enhanced thermal cycle reliability for harsh environment or mission critical applications.

Projects included in this alternate solder alloy research thrust include evaluations of microstructure and mechanical properties for various solder alloys and surface finishes. The work typically encompasses characterizations for both individual solder balls wetted to a surface finish of interest as well as components assembled onto test boards for second level reliability comparisons through thermal cycle or mechanical testing. The performance of the alternative lead free alloy solder joints is often compared to that of the common SAC305 alloy or eutectic SnPb, as appropriate.

MAT7A. High Reliability Pb-free Solder Alloys: Thermal Cycle Dwell Time Effects

Companies responsible for electronics in such as those found in the military/aerospace, energy or lighting industry are actively searching for solder alloys that would provide exceptional interconnect reliability in their demanding applications. In recent years, the AREA Consortium has actively evaluated the thermal cycle reliability of many commercially proposed alternative Pb-free alloys. These comparisons have typically been done with a single thermal cycle profile which doesn't enable extrapolation to thermal cycle conditions that may exist in the field. This study will explore the mechanical behavior of select high reliabiility alloys under conditions of various elevated temperature dwell times including correlation with microstructural observations. The results of these measurements will inform future planned thermal cycle testing of realistic component test vehicles using popular high reliability solder alloys at various cyclic conditions.

MAT7F. Characterization of Bi Mobility in Low-Melt BiSn Mixed Solder Assemblies

Key suppliers of large body BGA components such as microprocessors are promoting the use of low melting point solder for board attachment to minimize the impact of temperature induced warpage on assembly yield and package reliability. Board assembly with low melt solder paste will inevitably require mixed solder assembly for some BGA components such as commodity memory parts that will necessarily be sourced with SnAgCu based BGA balls. This project characterizing mixed solder joints formed with SAC305 BGA spheres joined with BiSn eutectic solder paste started in 2019 examining the degree of mixing as a function of reflow profile and the relative paste to ball volume ratios. 2020 efforts will quantify the kinetics of further Bi diffusion into the attached SAC solder ball as a function of time and temperature. Opposing or additive atomic fluxes of Bi driven by applied electric current during the elevated temperature exposure will also be measured through quantitative microstructural observations.

MAT7H. Reliability of Low Temperature Solder BGA Joints

Previous consortium LTS reliability evaluations focused primarily on mixed alloy solder joints (i.e., SAC305 BGA with BiSn solder paste). Full implementation of LTS will however include homogenous solder joints in which the BGA packages will be provided with LTS alloys matching the board assembly paste alloy. This project will evaluate the thermal cycle reliability of such homogenous LTS BGA joint using a 1.0mm pitch BGA memory package. Two low temperature solder (LTS) alloys, eutectic BiSn1Ag alloy and an off-eutectic BiSn alloy, will be thermal cycle tested to failure in BGA solder packages.

MAT7I. Thermal Cycle Reliability of Low Temperature Solder BGA Joints

The use of low melting BiSn eutectic based solders by early adopters will generally entail fully eutectic BiSn solder joints for BTC components and BiSn mixed assembly for SAC305 BGA components. For custom (non-commodity) BGA components it may be feasible and economical to supply the BGA interconnects with fully eutectic BGA solder balls. Thermal cycle reliability testing of fully BiSn(Ag) solder joints (*i.e.*,

BiSn(Ag) spheres on BiSn(Ag) paste) was initiated in 2019; cyclic testing will continue into 2020. This reliability test uses a new AREA test board that includes BGA228, BGA208, BGA196 and one stitched RLDRAM memory part all balled with BiSn eutectic 1%Ag solder alloy spheres. All BGAs were attached with the same composition past, either BiSn1Ag or the Nihon Superior LT1 proprietary alloy. BGA pitches on test include 0.5 mm, 0.8 mm, and 1.0 mm. Two thermal cycle profiles are in progress: 0/100C and -40/125C. And additional cell of 20 to 80C cycling at a member company facility will be added in 2020.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. Our Principals often require standardized accelerated life testing for product qualifications. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

REL3E. Vibration Reliability of High Performance Solder Alloys used with SAC305 BGAs

Early implementation of alternative solder paste alloys will inevitably encounter BGA components in the BoM that must be sourced with SAC305 solder balls. Since most such alternate paste alloys are SnAgCu based, the mixed solder joints formed with these pastes and SAC305 BGA balls fully reflow at assembly and thus form essentially homogenous, but now lightly alloyed, solder joints. Prior consortium vibration testing of high reliability alloys therefore investigated such mixed solder joint configurations but with limited success. Failures were predominately observed in the copper traces connecting the BGA pads. No conclusions could be drawn regarding relative solder alloy performance. The vibration test board has since been redesigned for 2020 with a single BGA208 component (0.8mm pitch) having solder mask defined pads. Preliminary vibration testing has confirmed solder failures. Using this test board design several high reliability alloys will be vibration tested in the mixed alloy joint configurations. Harmonic vibration will used at 2G and 4G accelerations. Selected paste alloys will include Innolot, Senju M794, Cyclomax, Violet and Maxrel Plus.

REL8A. Wafer Level Chip Scale Package (WLCSP) Interconnect Reliability without Post Chip Join Cleaning

In a 2019 consortium study, WLCSP devices with 0.30mm thick die were found to be quite robust in thermal cycle when appropriately underfilled. According to best practices, the prior test parts were cleaned prior to device underfill to promote encapsulation integrity. Given the acceptable reliability of these parts in the underfilled state, a 2020 follow-up study will investigate elimination of the post chip join wash step as a manufacturing cost savings option. This new project will also explore the thermal cycle reliability limits of larger body WLCSPs (up to 12 mm) using electrically stitched devices in a -40/125C thermal cycle. The same WLCSP body sizes (4, 5, 6, 8, 10, 12 mm square) will again be tested. WLCSP assembly will either use a flux dip or paste dip chip join process. Low CTE laminate material (Elite EM526) and standard FR-4 board material will again be used for the test board. All devices will be underfilled with Loctite 8803S.

REL9A. Mixed VIPPO (Via-In-Pad, Plated Over) Array Induced BGA Solder Defects

Solder joint interfacial separation at BGA joints above Via-in-Pad Plated Over (VIPPO) connected solder pads during second reflow events has been a persistent problem for lead free BGA components. Experimental investigation of this phenomenon has been underway in the consortium research portfolio for several years now using a custom test board design. This test board emulates the behavior of relatively thick boards (>110 mil) for complex network/server applications. It includes BGA footprints with varying VIPPO/non-VIPPO densities and intermixing configurations with and without backdrilling. Test components include two standard BGA memory packages and two different 1.0 mm pitch lidded BGA parts with 55 mm body size. The experimental phase of this project is essentially complete. Key observations have been made regarding VIPPO design attributes as well as solder reflow environment, flux coverage, and solder alloy selection. 2020 efforts will focus on 1) physical characterization of the response of the test board surfaces to reflow temperature exposure using available optical methods (e.g., shadow Moiré interferometry and digital image correlation) and 2) quantifiable correlations of such measurements to the previously observed VIPPO solder defect rates.

REL10B. Effect of Laminate Material on BGA Drop Shock Reliability

Prior AREA research into the drop shock reliability of a BGA208 component often revealed parallel and interactive failure mechanism operative in the laminate material as well as the BGA solder joint. Despite the final electrical failures occurring in the corner solder joints, this parallel laminate crack path was seen to dissipate additional energy during the repetitive drop shock events. Moreover, it contributed to deflection of the ultimate solder joint crack, extending the critical path length. Given the participatory role of the laminate in the failure process, it is hypothesized that laminate material properties (*e.g.*, fracture toughness) can contribute to the measured BGA drop shock reliability. The drop performance of test boards of six different laminate materials will be measured using BGA interconnects of a new high performance solder alloy compared to conventional SAC305 solder. Laminate materials include several

high performance (low loss) materials compared to our more commonly used 370HR baseline material.

REL15B. Power Cycle Reliability of QFN Packages

Wirebond QFN packages fabricated with resistive test die had been previously tested (2017) in a constant current power cycle using the APL power cycle test apparatus. The package was a single perimeter row 12.0 x 10.5 mm body with a 0.4mm lead pitch. Each die contained eight resistive elements to emulate functional hot spots on a die. The body of these test packages included a snap on cover leaving a hollow package body. Consequently, cyclic power from the die was not being dissipated in a realistic fashion through the QFN body. Power cycle testing drove die bond delamination failures rather than expected solder interconnect failures. In 2019, similar open body QFN packages with thermal test die was gloptopped with a filled epoxy encapsulant to create a testable package more structurally representative of an epoxy overmold QFN package. These QFNs were placed on power cycle test in 2019. The packages with improved thermal path are proving far more robust in power cycle than the original snap top packages. No failures have yet been observed. Cycling will continue in 2020 in an attempt to force solder interconnect failures.

REL15D. BGA Reliability with Local Die Heating in Environmental Thermal Cycle

Traditional environmental thermal cycling of hardware is being supplemented with a superimposed constant current power cycle. The intent is to provide a more realistic thermal mechanical reliability stressing through the inclusion of transient temperature gradients similar to those produced in the operation of functional electronics. This test part used for this study is a 45x45 mm laminate BGA package attached to a printed circuit test card. The package contains a 15.4 x 15.8 mm flip chip with a main heater for uniform heating as well as three local individually controllable “hot spot” heaters and five temperature sensors. The BGA solder joints along the package perimeter and those beneath the flip chip comprise five electrical continuity test nets to be monitored for BGA failure during the combined cycling. The APL custom designed power cycle test circuit is used to supply a constant current that drives the main chip heater at the time intervals of interest. Several years of reliability data have been collected with these parts using an environmental thermal cycle of -40 to 90 C, (135 minute period) and a superimposed +30 C power cycle (15 minute period) with uniform die heating. A follow-up test using the same environmental thermal cycle but with single corner heating of the die was begun in 2019 but is having only limited success because of unreliable die heaters. The final 2020 increment of this project will additionally explore the use of die edge heaters rather than individual spot heaters.

REL17A. Electromigration Behavior in Low Temperature BiSn Based Solder Joints

Prior AREA research has shown a marked mobility of Bi atoms in mixed BiSn-SAC305 solder joints under the influence of applied electric current. Significant migration of Bi to the anode side of the solder interconnect has been observed in mixed (or hybrid) joints and is often accompanied by substantial intermetallic growth. While no electromigration induced void formation has been observed in such mixed joints, vacancy coalescence and void formation does occur at the cathode of homogenous BiSn based

solder joints (e.g., LGA joints). This project will investigate electromigration void formation and failure kinetics in homogenous BiSn solder joints. A custom test package will be designed to limit the self-heating of the package and control the failure location under an applied electric current. Tests will be run with multiple current densities at several different ambient temperatures. Several industry available low temperature solder alloys based on the BiSn eutectic system will be included to explore the impact of common alloying elements.

REL17B. Sequential Electric Current and Thermal Cycle Testing of BiSn|SAC Mixed Solder Joints

AREA studies have observed the dynamic nature of the Bi strengthening phase in low-melt solder joints. Marked migration of Bi phases can be observed under sustained electric current flow particularly at elevated temperatures. This Bi redistribution will affect the accommodation of cyclic strain in the joint during an environmental thermal cycle. A 2019 experiment in which a constant electrical current was supplied to hybrid SnBiAg and SAC305 solder joints during a superimposed thermal cycle did not however reveal a substantial reliability impact of such current flow. This 2020 follow-on investigation will instead monitor the thermal cycle reliability of test boards which were previously exposed to a constant current for an extended time at elevated temperature. Because of the elevated temperature the resulting current damage is expected to be greater. Subsequent exposure to an environmental thermal cycle may then show an exaggerated failure rate. This experiment will be run with known components on the TB2019 ATC test board so that prior reference data exists for comparison.

Assembly Process Development

By virtue of its access to state of the art surface mount manufacturing equipment, the AREA Consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy member access in addition to the final project reports (http://www.uic-apl.com/databases).

APD1D. Solder Dispensed Repair of Low Volume Print Deposits

Previous consortium research explored the reliability consequences of low volume solder paste print deposits on both BGA and BTC components. Intentionally created low volume deposits with reduced stencil apertures at key risk sites was able to demonstrate both negative and positive effects of paste print defects. Low volume deposits were the most detrimental for Bottom Terminated Components such as LGA parts, producing measurable reductions in thermal cycle reliability. To mitigate this problem, Koh Young is now offering solder paste inspection tools with an on-board solder paste dispenser to replenish low volume deposits as they are detected. A Koh Young 8030-3 SPI tool with such a solder jet dispense head has been installed in the APL for evaluation trials. Using a previously designed test board/stencil combinations to produce controlled print defects, individually dispensed print reworks will be selectively programmed for product quality and reliability evaluation. A standard SAC305 solder paste will be used

APD2D. Thin Die Assembly with Flexible Substrates

The AREA consortium had previously examined various die interconnect methods for flexible substrate materials with limited temperature capability. While several viable methods were demonstrated, all used die of fairly conventional thickness (300μm or greater). In the 2020 iteration, ultra-thin die (<50um) will be used for assembly trials to maximize flexibility of the final assembly and be more representative of actual hybrid flexible electronic applications. Joining trials of thin die shall explicitly include area selective laser soldering using the latest prototype laser tool being defined in the APL. Comparisons to conventional mass reflow soldering methods will be made where appropriate. Thin test die are anticipated to further include early trials of Optomec printed copper test circuitry used to complete test circuits on the available flex substrates at joining. Device underfill materials will be considered as indicated by robustness testing of the attached devices.

APD 4C. Rework of Underfilled BGA Components using Milling Removal

Periodic rework of BGA components (i.e., removal and replacement) is a necessity for most surface mount assembly manufacturing lines. The process for removing soldered components, site dressing and re-soldering is fairly well established and dedicated tools for this purpose are readily available. The need for added interconnect robustness in many applications has increased the practice of underfilling components after solder attach with filled epoxy materials. BGA component rework after such underfill encapsulation becomes significantly more challenging. When solder joints are fully encapsulated simply melting the solder joints does not release the part from the board. AirVac, a well-known provider of rework manufacturing tools, has recently been promoting the practice of machining off defective components from a board if they are fully underfilled. This capability is offered as a built-in tool option in their AVX-250 rework system. AirVac has committed to provide such a tool to the APL for consortium evaluation. Pending delivery of such a tool, this project will explore the process of milled component rework, establishing for instance how close to the board surface must the underfill be milled to get a

reliable reconnection. Similarly, the robustness of the processes for site dress and resoldering of new BGA components to milled encapsulant surfaces will be explored.

Advanced Semiconductor Packaging

The end of decades of successive scale reductions by the silicon semiconductor industry has not diminished the industry drive for increased functional density of microelectronics. Progressive semiconductor scaling has been replaced by an aggressive push for more heterogeneous integration of device functions onto common packages. This new consortium research thrust will address unique package designs and assembly processes mandated by the various heterogeneous package structures of interest to consortium members and their product development teams. Previous consortium research has demonstrated that the reliability of interconnects in multi-function packaging structures can interact in complex ways. REL17A. (System in Package Interconnect Reliability) revealed for instance that the location and failure rate of board level interconnects is markedly affected by the locations of multiple devices on the topside of the package. The complexity of heterogeneous packaging structure foreseen by the IEEE Heterogeneous Integration Roadmap hints that the interconnect failure mode and rate will be often difficult to anticipate at the package design stage. Empirical reliability confirmation of any given package design will be a critical element of the product development cycle.

PKG1A. Package Integration of Multiple Silicon Chiplets

This initial project will explore the assembly process challenges for multiple die packages using representative test hardware including ten or more chiplets per package. Key variables to consider will be die interconnect pitch, die thickness, die placement spacing, substrate technology, and underfill selection. While package level device integration for AREA members is anticipated to ultimately accommodate various device technologies (GaN, SiC, etc), this first evaluation will be limited to silicon chiplets. The project is planned for a fourth quarter start pending availability of chiplet test hardware anticipated from key member companies. Interconnect reliability monitoring will be a function of available test hardware.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and useful manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Projects may require the staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.