ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2019 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and electronic assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to engineering topics directly applicable to manufacturing challenges. In every case, the objective is to provide AREA Principals with meaningful results that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a consortium website will be maintained with on-demand content (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals. Longer term reliability evaluation projects may extend into subsequent plan years as needed to complete testing. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities and faculty expertise as needed.

The primary focus for 2019 will be the careful execution of the projects outlined in this document. History indicates that additional topics will be added throughout the year as our capabilities develop, member interests evolve and materials are provided. The research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

MAT1C. Capillary Underfill and Edge Bonding of BGA Components

As the use of minimalist packaging schemes such as wafer level CSP migrates to larger and larger devices, interest in component underfill encapsulation for improved thermal cycle reliability has increased. The use of underfill encapsulation for these board level attachments requires not only selection of the appropriate material but also specification of the extent of underfill required. In many cases, edge bonding and corner bonding may well be adequate. The anticipated benefits of partial encapsulation schemes include reduced process time and materials consumption. Enhanced reworkability is also a commonly cited advantage over full underfill encapsulation given the easier component removal and site dress with partial underfill configurations. This study will compare the effectiveness of the reliability enhancement provided by several recent material offerings applied to a variety of area array packages: CVBGA208, CVBGA432, CABGA208, CTBGA228, PBGA515, and BGA2116. Package body sizes range from 12mm square to 31mm square. Two capillary underfill materials (United Adhesives UF1230 and Namics SUF1570-2) and three edge-bonding materials (Namics SUF1583-19, ZYMET UA-3307-B and ZYMET UA-2605) will be evaluated. All are heat curable; only one (UA-2605) is advertised as being reworkable. This study will focus solely on assembly process and thermal cycle reliability performance (-40 to 125C); no other mechanical or shock loadings will be included.

MAT2D. Pad Cratering Behavior in Cyclic Bend Test by Laminate Material

Several member companies continue to be plagued by pad cratering of laminate materials under critical large components during assembly induced board strains. This project revisits a previously defined consortium test method for comparing pad cratering tendencies among different laminate materials using a cyclic four point bend test. In this vehicle two BGA components are assembled along the axis of board bend in order to impose tensile strains along the outer BGA solder joints which promote laminate pad cratering especially under the corner solder joints. Test traces emanate from the corner joints to allow electrical monitoring of the completed cratering event. In the present study, the pad cratering tendency

of several high performance laminates such as Megtron 6 and Nelco 4800 will be compared to our commonly used 370HR laminate material.

MAT3B. Electroless Palladium, Autocatalytic Gold (EPAG) Surface Finish

The EPAG board finish (electroless palladium, autocatalytic gold) is a direct Pd finish on copper with an optional Au layer. Its ability to deliver thicker gold layers enables wire bond connections as well as solder assembly. This project will examine the solder joint reliability consequences of this new finish using a newly designed test board 2019A. The board will be sourced with EPAG, ENIG and bare copper finishes and each version assembled using conventional SAC305 solder. All will be thermal cycled at -40/125C for a direct reliability comparison among these finishes. Drop shock performance will also be investigated using an EPAG version of the 2019 drop test board with a BGA196 package.

MAT4B. Graphite Pad Thermal Performance

This ongoing research program evaluates the performance of various thermal interface materials intended for heat sink applications. Typically candidate materials are suggested by member companies and may include thermal greases, putties, and thermal pads. Using a precision thermal rod test apparatus, thermal resistance is measured as a function of bondline thickness, and where appropriate, heat sink load. The 2019 interface materials list includes several graphite thermal pads (such as Jones 21-1500, Allied SO1500, Nolato 9610 and Nolato 9450 pads). The reliability of a select subset of the candidate interface materials will compared, initially through cyclic mechanical shear testing, and selectively with accelerated thermal cycling. (These materials are electrically conductive and not suited for the capacitance based reliability test method of MAT4C.)

MAT4C. Reliability of Thermal Greases for Heatsink Applications

The advertised performance of thermal interface materials for heat sink applications is typically reported as thermal resistance measured in the as-applied state. The stability of this condition may however be suspect, with thermal performance degrading with system operating hours. This on-going project monitors the stability of member selected TIM2 materials using a capacitance measurement across the TIM bondline. This custom test apparatus mimics the TIM bond to an aluminum heatsink. The prepared thermal interface is stressed in an environmental thermal cycle at individual sites having a range of different distances from the system neutral point. Thermal expansion mismatch between the aluminum heatspreader and the mated circuit board imposes a cyclic shear load on the TIM2 bondlines that can degrade the TIM thermal performance. Using the mathematical analog between capacitance and thermal conductance, the degradation of TIM performance is measured independently at each test site. TIM2 materials selected for 2019 evaluation include Laird T-Grease 2500, Nolato 9540 Grease and Joines 21-430SF Grease. A new test apparatus will be fabricated to test these materials using thin (0.25μm) bondlines.

MAT4D. Indium Metal TIM1 Materials and Processing

High performance processor and ASIC applications often demand the extreme thermal performance of fully metal thermal interfaces between the silicon die and metal heat spreader. Indium metal is a common choice, applied as a metal preform reflowed to attach the heat spreader to the die during module assembly. The fragility of the interfacial intermetallic formed when using Au metallizations on the silicon and heat spreader has proved to be a problem. Moreover, the indium TIM system is prone to excessive void formation during subsequent reflow events at the board level. This project will explore the viability of using Ag metallization for indium TIM connections, exploring the intermetallic formation, bulk microstructural features and multiple reflow induced voiding in the TIM layer.

MAT6 Series: Harsh Environment Electronic Interconnect

As electronics become integrated into higher temperature environments such as those associated with deep well drilling and distributed engine controls in the automotive and aviation applications, higher melting temperature and more thermally stable solder alternatives are being explored. In 2017, our harsh environment electronics thrust will include research on both die level and board level metallic interconnects critical for reliable high temperature electronics applications.

MAT6C. Sintered Silver Die Attach Materials

High temperature die attach materials are critical for the operation of next generation power electronics applications including those using wide band gap semiconductor devices such as SiC. These devices dissipate substantially more energy than conventional electronics. A metal based die attach system is typically required to provide sufficient thermal flux to remove the waste heat from these devices. Previous AREA research evaluated the sintering characteristics of a candidate sintered silver die attach materials formulated for pressure-less processing. Formulations with either micron scale particles or nanoscale particles were studied. The 2019 continuation project will include the evaluation of a new silver paste material. Experimental content will include paste printing characterization, sintering kinetics, and interfacial strength measurement, similar to the protocol used with previous materials.

MAT6H. Sintered Copper Interconnects

Several sintering copper paste materials formulated with nanoparticle copper have come available on the market. Because of the superior electromigration performance of all-copper interconnects, one targeted use for these copper pastes is the formation of fine pitch die level interconnects for higher power applications. This could be device attachment to a substrate or to another die to create thin die stacks. This project consists of early process trials for one such paste material, evaluating joint integrity as a function of sintering parameters. Copper bumped devices will be joined to copper pads on various substrate materials. Joining will be done in a formic acid reducing atmosphere. Process variables of interest include time, temperature and pressure of the sintering operation. The quality of the sintered

bond to the pad and bump surfaces will be of particular interest as well as increased density (reduced porosity) of the sintered copper structure itself. Possible methods to minimize sintered porosity may include evacuation before backfilling a formic acid environment, amount/time of formic acid exposure, peak temperature and/or time, and post sinter annealing.

MAT7 Series: Lead-Free Solder Alloy Evaluations

New lead free solder alloys with various alternative alloying elements are being routinely proposed in the industry as replacements (improvements) to the standard SAC305 alloy. Industry interests in recent years have been in 1.) low melting temperature solder alloys to minimize the assembly/reliability challenges posed by temperature induced component warpage and 2.) solder alloys with enhanced thermal cycle reliability particularly in harsh environments.

Projects included in this alternate solder alloy research thrust include evaluations of microstructure and mechanical properties for various solder alloys and surface finishes. The work typically encompasses characterizations for both individual solder balls as well as components assembled onto test boards for second level reliability comparisons through thermal cycle or mechanical testing. The performance of the alternative lead free alloy solder joints is often compared to that of the common SAC305 alloy or eutectic SnPb, as appropriate.

MAT7A. High Reliability Pb-free Solder Alloys: Effect of Bismuth Content

Companies responsible for mission critical electronics such as those found in the military/aerospace sector are actively searching for solder alloys that would provide exceptional interconnect reliability in their demanding applications. Many such applications have been out of scope of product environmental regulations banning the use of Pb and consequently have continued to use SnPb eutectic based solders. Now considering a transition to Pb-free assembly solutions, they desire to bypass the common SAC305 solder selection and move directly to a higher reliability alternative. In recent years, the AREA Consortium has actively evaluated the thermal cycle reliability of many commercially proposed alternative Pb-free alloys. The improved performance of most such alloys is dependant on varying levels of solid solution strengthening elements such as Bi or Sb. This project will systematically investigate the consequenses of increasing Bi content from approximately 1 to 6 weight percent. Experimental content will include detailed microstructural analysis and mechanical behavior assessment in both the assembled state and after accumulation of thermomechanical fatigue damage.

MAT7F. Characterization of Low-Melt BiSn Mixed Solder Assemblies

Key suppliers of large body BGA components such as microprocessors are promoting the use of low melting point solder for board attachment to minimize the impact of temperature induced warpage on assembly yield and package reliability. Board assembly with low melt solder paste will inevitably require mixed solder assembly for some BGA components such as commodity memory parts that will necessarily

be sourced with SnAgCu based BGA balls. This project will characterize mixed solder joints formed with SAC305 BGA spheres joined with BiSn eutectic solder paste. The degree of mixing will depend on the reflow profile and the relative paste to ball volume ratios. Characterization will include microstructural evaluations as well as mechanical property measurements including solder joint shear strength. Of critical interest is the known fragility of BiSn eutectic solders joints in high strain rate loadings such as drop shock testing. We anticipate being able to identify the onset of brittle behavior with increasing strain rate using mechanical shear test of BiSn|SAC mixed solder joints over many orders of strain rate.

MAT7H. Reliability of Bottom Terminated Components attached with BiSn Eutectic Solder

There is a marked industry push to develop lower temperature board assembly processes using BiSn eutectic based solder pastes to minimize the temperature induced warpage of large body BGA packages during assembly. These BGA packages are consequently anticipated to be interconnected with mixed BiSn|SAC solder joints. Other (non-BGA) bottom terminated components (BTC) however will invariably be called out in the Bills of Material for functional product assemblies. BTC solder interconnects in such low temperature product will necessarily consist of the paste solder alloy only. This project will examine the reliability of BTC solder joints when fabricated with the Bi42Sn1Ag solder paste. Two popular BTC package types will be tested, the MLF100 (0.4mm pitch) and MLF72 (0.5mm pitch) with 12mm and 10mm body sizes, respectively. The 0/105C thermal cycle reliability evaluation will include various surface mount resistors ranging in size from 0603 up to 2512 having a paste-only SMT solder attach.

MAT7I. Thermal Cycle Reliability of Eutectic BiSnAg BGA Solder Joints

The use of low melting BiSn eutectic based solders by early adopters will generally entail fully eutectic BiSn solder joints for BTC components and BiSn mixed assembly for SAC305 BGA components. For custom (non-commodity) BGA components it may however be feasible and economical to supply the BGA interconnects with fully eutectic BGA solder balls. This project will explore the thermal cycle reliability of fully BiSn(Ag) solder joints (*i.e.*, BiSn(Ag) spheres on BiSn(Ag) paste). A new test board will be designed that includes BGA228, BGA208, BGA196 and one stitched RLDRAM memory part all balled with BiSn eutectic 1%Ag solder alloy spheres and attached with the same composition paste. BGA pitches include 0.5 mm, 0.8 mm, and 1.0 mm. Interconnect reliability will be evaluated using two thermal cycle profiles: 0/100C and -40/125C to determine the thermal cycle acceleration factor for these low melting BGA joints.

MAT8E. Conformal Coat Evaluation with Ag Migration Coupons

Electronic assemblies and components, especially silver containing SMD resistors, can fail when IT equipment is installed in environments conducive to sulfur corrosion. Various conformal coating materials have been proposed as a means to protect board assemblies against environmental corrosive agents such as carbonyl sulfur and H_2S. An efficient method to evaluate the effectiveness of conformal coatings in protecting against sulfur corrosion may be to coat a thin film silver sensor (~800 nm thick) and

expose it to a Flowers-of-Sulfur (FoS) test environment. An accurate four-wire resistance measurement of the silver sensor can be made in situ, at regular intervals during the FoS exposure. The reduction in silver film thickness due to corrosion loss is inversely proportional to the measured resistance and thus can be determined as function of FoS exposure. In this project, silver sensors will be coated with different conformal coatings (initially six) at different thicknesses and subjected to FoS exposure. Five of these coatings have been previously evaluated on AREA reliability test boards in long-term FoS test at three different temperature: 60, 80 and 105°C. This study will directly compare the FoS corrosion performance of the silver sensor test coupon to actual assembled test board performance and determine whether it provides a valid screening method for candidate conformal coating materials prior to actual hardware qualification testing

MAT9: Filled Polymer Electrical Interconnects

Conductive adhesives and other filled polymer systems provide an alternate method of electronic interconnect to reflow soldering. Such materials have a long history of use in low cost consumer goods where product design life is relatively short and reliability expectations modest. They typically produce relatively high impedance interconnects, but can nonetheless find application in higher grade electronics where very low assembly temperatures are an absolute necessity. In the fast growing realm of flexible electronics, many candidate substrate materials are incapable of surviving conventional flipchip soldering and therefore require the use of lower temperature electrical attachment technologies such as anisotropic conductive adhesives.

MAT9C. Self-Assembly Anisotropic Conductive Paste Joining Evaluation

A new low temperature component attachment approach had been introduced through the use of Self-Assembly Conductive Pastes. These materials incorporate randomly dispersed BiSn particles of a predetermined size and number density in a polymeric paste carrier material. This paste effects component joining when screened or dispensed to form a uniform film between components aligned with features on the underlying substrate. On heating, the BiSn particles melt into embedded liquid droplets that migrate to copper features on board and consolidate to form a psuedo solder joint between the board pad and the joining feature of the component above. The paste carrier material then polymerizes into a solid adhesive joint between the dielectric surfaces of the component and board effectively forming an underfill encapsulant. This process happens at relatively low temperatures so the use of these materials is anticipated for flexible electronic applications requiring relatively low I/O density. This project will explore the joining behavior of a single formulation of self-assembly paste with various pitch WLCSP components onto flexible substrates from a manufacturing process standpoint.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. Our Principals often require standardized accelerated life testing for product qualifications. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

REL3E. Vibration Reliability of Alternate Solder Alloy Solder Pastes

Any product implementation of an alternative solder paste alloy will quite likely encounter BGA components in the BoM that must be sourced with SAC305 solder balls. Since most such alternate paste alloys are SnAgCu based, the mixed solder joints formed with these pastes and SAC305 BGA balls fully reflow and thus form essentially homogenous, but now lightly alloyed, solder joints. This project examines the vibration reliability of such dynamically created, doped SAC solder joints. Various enhanced reliability solder paste alloys have been solicited from well-known suppliers. Examples include Innolot, M794, Violot, and Cyclomax among others. These pastes will be used to attach CTBGA208 dummy components supplied with conventional SAC305 solder balls. The vibration test board includes eight CTBGA208 placements aligned along a central line of board flexure. After characterizing the harmonic vibration modes of the assembled test board, vibration acceleration levels required to generate solder joint failures in an acceptable time interval (~hours) will be determined. Solder joint reliability of the BGA208 mixed solder joints will be compared among the various paste compositions.

REL8A. Wafer Level Chip Scale Package (WLCSP) Interconnect Reliability

Motivated by reduced packaging costs and increased functional density, the use of wafer level packages in electronic assemblies continues to grow. Due to interconnect reliability limitations however, wafer level chip scale packages (WLCSP) have typically been limited to small die (<5 mm body sizes). This project will explore the thermal cycle reliability limits of larger body WLCSPs (up to 12 mm) using electrically stitched devices in a -40/125C thermal cycle. A range of WLCSP body sizes (4, 5, 6, 8, 10, 12 mm square) will be tested, all with 0.3 mm thick die. Reliability performance on a low CTE laminate material (Elite EM526) will be compared to that on a more standard FR-4 board material. The largest body parts (10 and 12 mm) will include underfilled and non-underfilled test cells.

REL9A. Mixed VIPPO (Via-In-Pad, Plated Over) Array Induced BGA Solder Defects

The inability to reliably retain solder connections on VIPPO BGA pads through multiple reflows when a PCB design mixes non-VIPPO pads in the same component footprint is now widely recognized as a persistent reliability risk. Separation of the solder joint from the component pad occurs during second reflow above those BGA pads with underlying VIPPO structures. The specific design attributes of mixed VIPPO/non-VIPPO footprints that lead to the BGA joint separations is largely unknown, forcing many to simply eliminate the design flexibility of mixing these two board connection options.

This project explores the BGA solder defect rates associated with various combinations of VIPPO design attributes in the printed circuit board. Assembly test board designs for this experiment have been completed. These designs mix VIPPO and non-VIPPO pads in four different BGA package footprints with a wide variety of different geometric configurations. These test designs will explore the effects of relative VIPPO/non-VIPPO densities, package DNP location, and edge proximity. Test components include two standard memory packages as well as 55mm lidded BGA parts, all at 1.0 mm pitch. Boards will be fabricated with select VIPPO locations backdrilled (either shallow or deep) to see if shortening the underlying PTH reduces the reflow induced tensile loading on these VIPPO solder joints. A relatively thick test board (>110 mils) will be used to emulate the behavior of complex network/server applications. Reflow profile attributes will be explored paying particular attention to the temperature gradients produced during second reflow. A key objective of the study will be to identify PCB design rule guidelines for minimizing the occurrence of BGA interfacial separation when using various combinations of board via structures. The test boards used will be sourced with at least two different laminate materials to indicate the contribution of laminate properties on the design rules obtained. 2019 project tasks include evaluation of long buried vias under BGA pads. These structures have been found to produce solder joint separations on second reflow fundamentally similar to the VIPPO induced defects. These structures will be used to investigate sensitivities to reflow process parameters such as oxygen level and time above liquidus. The separation behavior of alternate BGA solder alloys (*e.g.*, SnPb, SnBi) will also be explored.

REL10B. Effect of Laminate Material on BGA Drop Shock Reliability

Prior AREA research into the drop shock reliability of a BGA208 component often revealed parallel and interactive failure mechanism operative in the laminate material as well as the BGA solder joint. Despite the final electrical failures occurring in the corner solder joints, this parallel laminate crack path was seen to dissipate additional energy during the repetitive drop shock events. Moreover, it contributed to deflection of the ultimate solder joint crack, extending the critical path length. Given the participatory role of the laminate in the failure process, it is hypothesized that laminate material properties (*e.g.*, fracture toughness) can contribute to the measured BGA drop shock reliability. The drop performance of test boards of six different laminate materials will be measured using BGA interconnects of a new high performance solder alloy compared to conventional SAC305 solder. Laminate materials include several high performance (low loss) materials compared to our more commonly used 370HR baseline material.

REL15B. Power Cycle Reliability of QFN Packages

Wirebond QFN packages fabricated with resistive test die had been previously tested (2017) in a constant current power cycle using the APL power cycle test apparatus. The package was a single perimeter row 12.0 x 10.5 mm body with a 0.4mm lead pitch. Each die contained eight resistive elements to emulate functional hot spots on a die. The body of these test packages included a snap on cover leaving a hollow package body. Consequently, cyclic power from the die was not being dissipated in a realistic fashion through the QFN body. Power cycle testing drove die bond delamination failures rather than expected solder interconnect failures. In 2019, similar open body QFN packages with thermal test die will instead be gloptopped with a highly filled epoxy encapsulant to create a testable package more structurally representative of an epoxy overmold QFN package. Power cycle testing will be repeated on these more realistic QFN structures while monitoring the solder interconnect reliability.

REL15C. Combined Power Cycle and Environmental Thermal Cycle

Traditional environmental thermal cycling of hardware is being supplemented with a superimposed constant current power cycle. The intent is to provide a more realistic thermal mechanical reliability stressing through the inclusion of transient temperature gradients similar to those produced in the operation of functional electronics. This test part used for this study is a 45x45 mm laminate BGA package attached to a printed circuit test card. The package contains a 15.4 x 15.8 mm flip chip with a main heater for uniform heating as well as three local individually controllable “hot spot” heaters and five temperature sensors. The BGA solder joints along the package perimeter and those beneath the flip chip comprise five electrical continuity test nets to be monitored for BGA failure during the combined cycling. The APL custom designed power cycle test circuit is used to supply a constant current that drives the main chip heater at the time intervals of interest. Sixteen PBGA modules have been under test since 2017 using an environmental thermal cycle of -40 to 90 C, (135 minute period) and a superimposed +30 C power cycle (15 minute period) with uniform die heating. This test will be terminated in 2019 and replaced with a hot spot test, *i.e.,* thermal cycling the BGA modules with a superimposed square wave power cycle at one corner of the die only.

REL17A. Electromigration Behavior in BiSn|SAC Mixed Solder Joints

There is strong industry interest in using BiSn eutectic solder pastes to enable reduced temperature board assembly processes. This necessarily creates mixed alloy solder joints for all solder bumped components such as BGA and CSP packages. Most often, these mixed solder joints will consist of component side SAC305 solder preform attached to the board with a reflowed BiSnAg eutectic structure. The volume ratio of the two will vary based on the pitch of the particular component. This project monitors the electromigration response of such BiSn/SAC305 mixed joints under sustained current densities ranging from 2 to 8 kA/cm^2 at various elevated temperatures (e.g., 85C or 105C). Initial experiments will be done using solder volume ratios (BiSn:SAC) of about 0.15. Early observations have revealed bismuth migration driven by both the electron wind force and the Bi concentration gradient in the Sn matrix. These effects

will be quantified over a range of assembly conditions and joint structures. Also of interest is the current induced disruption of the interfacial intermetallic structures at the anode and cathode interfaces.

REL17B. Combined Current and Thermal Cycle Reliability of BiSn|SAC Mixed Solder Joints

Several AREA studies have observed the dynamic nature of the Bi strengthening phase in low-melt solder joints. The migration of Bi phases under sustained current flow can be particularly extreme. This Bi redistribution will necessarily affect the accommodation of cyclic strain in the joint during an environmental thermal cycle. The effect on fatigue lifetime is unknown. This project will compare thermal cycle reliability of BiSn mixed solder joints with and without electrical current flow for a variety of BGA component types. Initial experiments will be sequential; current induced migration followed by ATC test. If initial results warrant, thermal cycle testing with the simultaneous application of constant current will also be explored. Such simultaneous stressing will require some test apparatus development and so may extend into the following year.

REL18A. Event Detection vs Resistance Monitoring for Underfilled Component Failures

A longstanding challenge in the thermal cycle testing of underfilled components is accurately identifying the timing of individual interconnect failures. Standard testing practice calls for event detection on electrical continuity nets through the board attachment solder joints. The presence of underfill encapsulant however maintains these solder joints in compression and can therefore suppress the event signals associated with solder joint thermal fatigue cracking. A better approach may be to monitor any drift in the total net resistance over time. TB2014U test boards have been populated with BGA208 and BGA228 stitched components (among others). These will be underfilled with Namics SUF1570-2 and subjected to -40/125C thermal cycling. Continuity test nets will be monitored with both event detection and net resistance data logging. Failure rate results from these two approaches will be directly compared for the various component types. Non-underfilled controls will be included.

Assembly Process Development

By virtue of its access to surface mount manufacturing equipment, the AREA consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy and quick access in addition to the final project reports (http://www.uic-apl.com/databases).

APD3C. Copper Coin Board Assembly and Reliability

The consortium will take a first look at circuit board assemblies with embedded copper coins for improved thermal performance. These structures consist of slugs of copper laminated into openings of the circuit board, often electrically grounded through electroplated connections to the PCB ground planes. These copper features would be strategically positioned under high power SMT devices and serve to extract additional heat from the package. Of interest in this project will be any unique SMT assembly attributes as well as identification of characteristic failure modes of the assembled coin structure in thermal cycle. This first steps approach will use small coupons of member company supplied product boards rather than custom designed test vehicles.

APD8B. Vacuum Reflow Induced Solder Bridging in BGA/CSP Components

A previous consortium evaluation of in-line vacuum solder reflow has shown this process to be quite effective in reducing solder void levels in the thermal pad connection of QFN packages. Extreme vacuum levels (<20Torr) are not required to impart this improvement. The solder void ejection response in smaller volume joints however appears to be different than that for large area thermal joints, particularly in the spherical shaped joints of BGA and CSP package designs. This study will systematically investigate the consequences of vacuum reflow on area array solder joints of varying pitches. Particular attention will be paid to the propensity of these packages to create solder bridging between adjacent joints during the application of vacuum.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and useful manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Projects may require the staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.