AREA Consortium

Dear Members,

Hopefully you have noticed that we are now sharing some brief consortium updates through a monthly E-news bulletin. The intent is to provide concise but regular snippets of consortium news. Please contact glenn.ackerman@uic.com if you are not receiving these e-mail bulletins* (and would like to). I do however still like the option for sharing visual and graphical content on individual projects afforded by the Newsletter format you're reading now so I will continue to periodically send out these high level articles as well.

Another innovation: traveling consortium meetings. We noticed that member attendance at our summer meetings never quite matched that we were getting at the early spring and fall meetings. For the last several years we've been experimenting with various options to make this mid-year meeting more useful or at least different somehow. Earlier this month, we hosted a test meeting remote from our usual Binghamton University venue. Research project status updates were shared at the NextFlex facility in San Jose, CA with targeted invitations to member company employees residing in west coast locations. Reasonably successful, we thought. We may yet consider other remote locations in future years if we can locate viable host facilities in productive locations.

Sincerely,

Jim Wilcox

Consortium Manager

* *This would be the case if you've previously Unsubscribed to any other Universal Instruments automated mailings.*

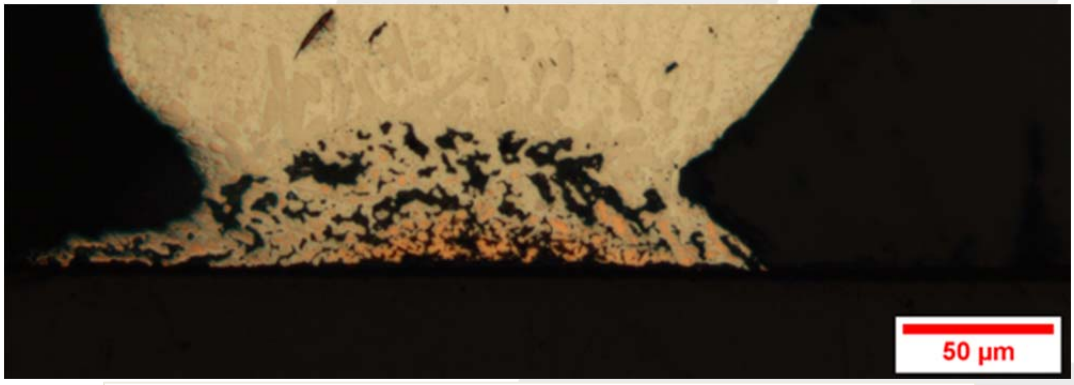
May consortium meeting at NextFlex facility in San Jose, CA.

MAT6G. Automotive (Engine Control) Solder Alloy Reliability Study

Five alternate alloy solder pastes, designed for elevated temperature applications such as automotive or aviation engine control electronics, were acquired for a comprehensive thermal cycle reliability evaluation. These solder pastes, along with a SAC305 reference paste, were used to assemble test boards containing LGA, BGA, PLCC, QFN, SMR, SOIC and QFP componentry. Included in the build were mixed alloy BGA (*i.e.,* SAC305 solder balls + alternate paste) and 'pure' alloy BGA (*i.e.,* matching solder ball and automotive paste). All test boards have been electrically tested and inspected using x-ray imaging. Cross-sectional analyses of representative samples are pending. The five test cells are being cabled in preparation for a -40 to 150°C harsh environment thermal cycle.

Flexible Hybrid Electronics: Soldering to Copper Based Ink Circuitry

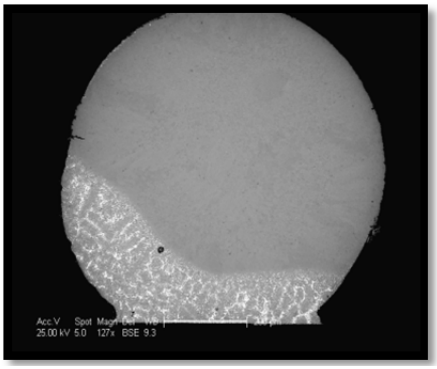
A common vision for flexible hybrid electronics product is a low cost polymer film populated with thin flexible devices all connected by screened ink circuitry. Supporting that vision, soldering to ink circuitry is being explored as a key element of the temperature sensitive flexible substrate assembly project. WLCSP devices with SAC405 bumps were bonded to copper based ink circuitry using the Finetech die bonder. Various reflow times were run to explore the effect of added diffusion time on the solder/ink joint microstructure. That microstructure was seen to be significantly altered, from minimal solder/ink interaction formation to significant IMC growth in both the SAC solder and the ink. An extreme example is shown were the solder has significantly mixed with the ink copper particles. The electrical and mechanical implications of such microstructures are being examined.



SAC405 chip bump reflowed on a copper based ink trace for 300 seconds.

MAT7F. Low-Melt BiSn Mixed Solder Reliability Study

Reliability test boards populated with SAC305 BGA and CSP as well as LGA and QFN componentry were assembled using one of two 'low-melt' BiSn eutectic based solder pastes (T_m= 139°C). Test populations were assembled at peak reflow temperatures of 150, 175 or 200°C, all well below typical Pb-free solder reflow temperatures. These test cells along with one extended reflow time cell are intended to explore solder mixing effects on BGA reliability as well as baseline BiSn reliability for the bottom terminated components. Post assembly x-ray imaging and electrical tests were encouraging, with all parts testing electrically good and solder joint voiding within acceptable limits. Cross-sectional analyses are still pending. Limited solder mixing behavior, similar to that reported at the March meeting (below), is expected. The test assemblies have been placed in an environmental chamber for accelerated life testing. A less aggressive temperature thermal cycle (-40 to 105°C) has been selected to avoid unrealistic damage mechanisms at high homologous temperatures for the BiSn alloy. At this writing 200 cycles have been completed.

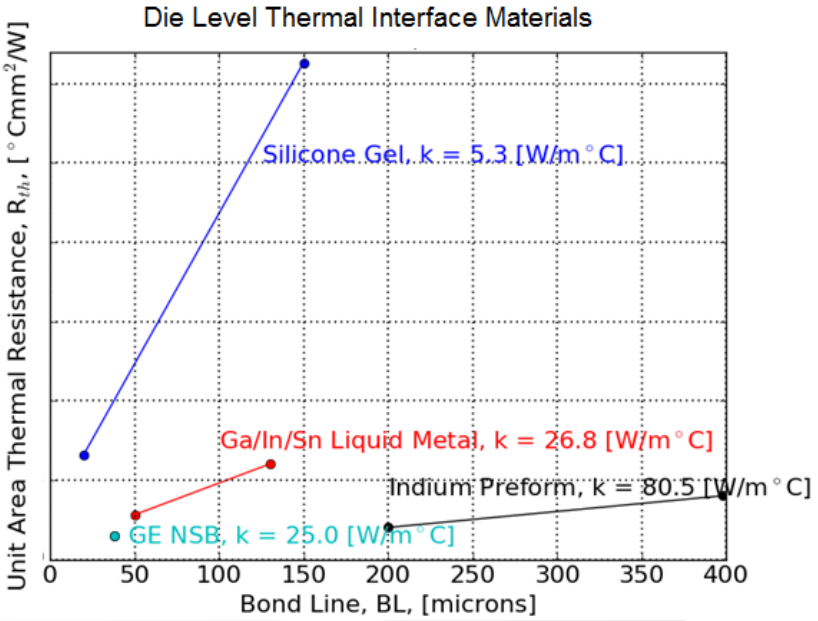


Limited mixing of BiSn eutectic solder and 20mil SAC305 solder ball (200C).

Test Group	Paste Alloy	Peak Reflow Temperature	Time Above Liquidus
1	42Sn58Bi	175 C	60 sec
2	42Sn57Bi1Ag	150 C	60 sec
3	42Sn57Bi1Ag	175 C	60 sec
4	42Sn57Bi1Ag	200 C	60 sec
5	42Sn57Bi1Ag	175 C	160 sec

MAT 4D: High Performance Die Level Thermal Interface Materials

A figure-of-merit comparison has been completed for several high performance die level thermal interface materials. The TIM1 candidates tested included two commercially available thermal solutions (indium solder and a silicone gel) and two more developmental solutions (a copper nano-spring bonding (NSB) developed by GE Research under the DARPA Nano Thermal Interfaces Project and a GaInSn liquid metal). Initial thermal characterization consisted of thermal resistance and thermal conductivity measurements using the APL thermal rod tester. Measured thermal resistance values of the three metallic solutions were all ≤ 5°C mm^2/W. The figure below illustrates these results for the four candidates TIMs. Noteworthy for the indium material is the insensitivity to bond line thickness (shallow slope), with thermal resistance < 5°C mm^2/W over a range of 200 to 400 micrometers. The thermal conductivities measured for indium and liquid metal both matched literature values well within the measurement accuracy (±6% for the solid metal indium, ±9% for the liquid metal). Only a single sample bond line thickness (50µm) was available for GE NSB case. Its thermal resistance was measured at 1.5°C mm^2/W, in good agreement with that of the GE developers.



Evaluating the long term stability of the thermal performance required testing in a representative use condition. Flip chip ball grid array (FCPBGA) packages that included a 15 x 15 mm thermal test die were assembled using silicone gel, indium and NSB TIMs. The time zero thermal resistances for these three FCPBGA modules were all measured to be ~12°C mm^2/W. Scanning acoustic microscopy revealed some voiding in the silicone gel interface. The module with indium showed delamination between the chip surface and indium. It is expected that minimizing the time above the melting point of indium would result in lower intermetallic compound growth between the indium and gold surface of the chip and thus reduce the thermal mechanical stress at this interface.

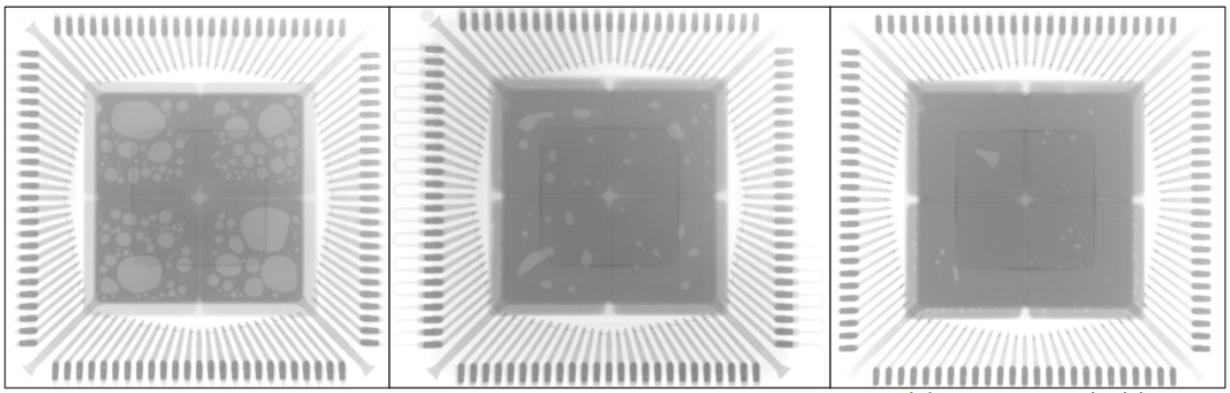
Intel processor module

In a second method, Intel Core i3 processor modules were disassembled and rebuilt using each of the four TIMs. The rebuilt processor module with the silicone gel experienced a 4°C drop in core temperature relative to the as-received thermal solution. This improvement was stable through 1000 thermal cycles of -40 to 125°C. The GaInSn liquid metal TIM applied to the Intel Core i3 resulted in a 9°C decrease in core temperature. However, after 100 thermal cycles of -40 to 125°C, the core temperature *increased* by 9°C. The Intel Core i3 modules assembled with indium and GE NSB produced core temperatures 6°C and 9°C cooler, respectively; values which remained relatively stable through thermal cycle.

AREA Consortium

APD8A. In-line Vacuum Reflow: Solder Joint Voiding Elimination

We are actively exploring the process characteristics of SMT solder reflow with the in-line application of vacuum. The vacuum reflow oven in the APL used for these experiments operates like a standard convective reflow oven but includes an automated vacuum chamber in the hot zone capable of evacuating the ambient pressure down to 1 Torr. Our initial reflow experiments have included evaluations of vacuum level and vacuum hold time and how these parameters affect QFN thermal pad voiding. Not surprisingly, the application of vacuum results in a reduction in overall QFN thermal pad voiding that quantitatively scales with the evacuation level and duration applied. The vacuum level and time required to achieve the desired results however was found to vary significantly with package size.



X-ray images of void levels in MLF100 parts soldered with reflow having (a) no vacuum, (b) 123 Torr vacuum with 20 second hold and (c) 13 Torr vacuum with 20 second hold.

Interestingly, we have observed that the vacuum pull-down and pressure restore rates may also be important factors affecting assembly yields. Rapid vacuum pull-down and/or pressure restore rates appear to be responsible for component shifting. Oven controls do allow for adjustment of these rates so their process sensitivities are being investigated. Other component types may impose additional process constraints. We have for instance observed in 0.4mm pitch WLCSP components that solder voids which often form in the BGA joints due to solder paste printing and reflow processes may expand to such an extent during the application of vacuum that the expanded solder joint bridges to neighboring solder joints. Once all such process and yield consequences unique to the vacuum reflow process have been identified, more systematic process windows for in-line SMT vacuum reflow will be mapped out.

MEMBERS ONLY

Additions to the AREA report archive …

Area Laser Selective Reflow Characterization – Basic Process and Interconnect Quality
by Luke Wentlent

Solder Joint Void Formation in LGA and QFN Assemblies
by Michael Meilunas