Dear Members,

Our June consortium meeting was held in conjunction with the iMAPS Advanced Technology Workshop on *Advances in Semiconductor Packaging*, exposing interested consortium members to a broad range of semiconductor packaging topics. We have similarly been exposing the AREA research portfolio to more first level packaging content. Most notable is the detailed study we've been running on die level copper pillar interconnects. Professor Eric Cotts (BU Physics) shared a little of this interconnect characterization work with an attentive audience at the recent CPMT ECTC conference.

In this issue you'll see that we're further increasing the breadth of our die attach capabilities. We've been actively comparing IR laser reflow chip join processes with conventional convection reflow process. And with our newly installed Finetech die bonder we have the opportunity to explore thermal compression bonding for these same fine pitch, large die interconnects.

Sincerely,

Jim Wilcox

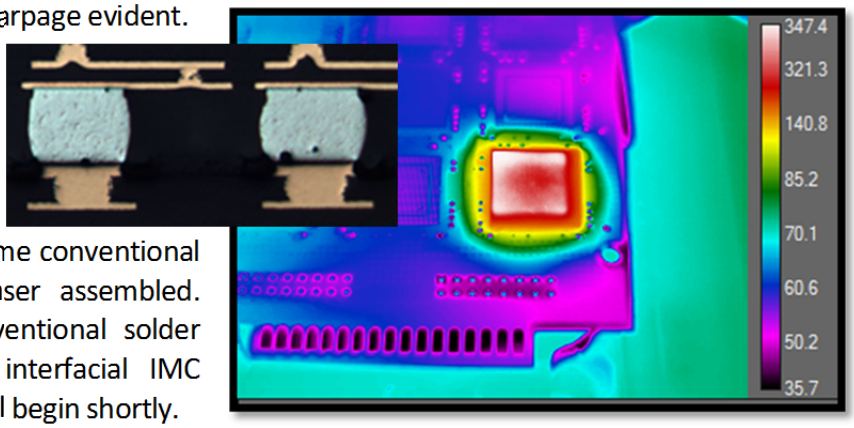
Consortium Manager

APD11A,B. Laser Selective Reflow Soldering

We've been actively exploring the electronic assembly capabilities of the Crucial Machines Area Laser Selective Reflow (aLSR) tool recently installed in the lab. With the 1 kW Nd-YAG laser operating in the near-infrared range, materials like Si or Cu readily absorb the IR energy and conduct heat to the solder joints, driving reflow in seconds. The laser light is directed using custom optics that allow for accurate application of the incident beam in various sizes and shapes. While the tool is primarily marketed for flip chip assembly, our interest is broader: to assess the joining process and interconnect quality for a variety of package types, to explore the full range of process parameters (laser power, exposure time, and beam size), and to identify novel applications.

Early work has focused on fully characterizing reflow profiles for flip chip and CSP assemblies. Using embedded thermocouples in conjunction with the tool on-board IR camera, we can monitor transient temperature gradients throughout the package over a range of laser parameters. Profiles were developed for specific packages to achieve appropriate peak reflow temperatures while managing gradients. The CSP packages used in this study exhibited a temperature difference of 50 to 80°C through the package body. As long as the entire package is within the laser beam, the heating is reasonably uniform, with little warpage evident.

Joining quality is being ascertained by mechanical shear testing and conventional microscopy methods. Preliminary observations are that, in addition to flip chips, some conventional package types can also be laser assembled. Joints generally displayed conventional solder microstructures. Studies on interfacial IMC formation and solder wetting will begin shortly.



Infrared image of a CSP package reflowed under a 15mm x 15mm incident laser beam; resulting joints in inset.

Should you have specific suggestions for the aLSR tool or have samples that you would like evaluated, please contact Dr. Luke Wentlent <luke.wentlent@uic.com>.

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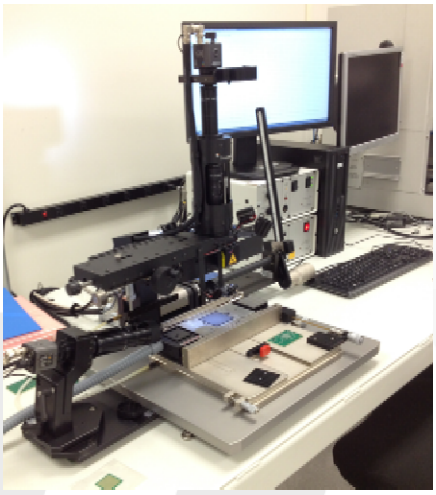
Finetech Fineplacer Pico bonder

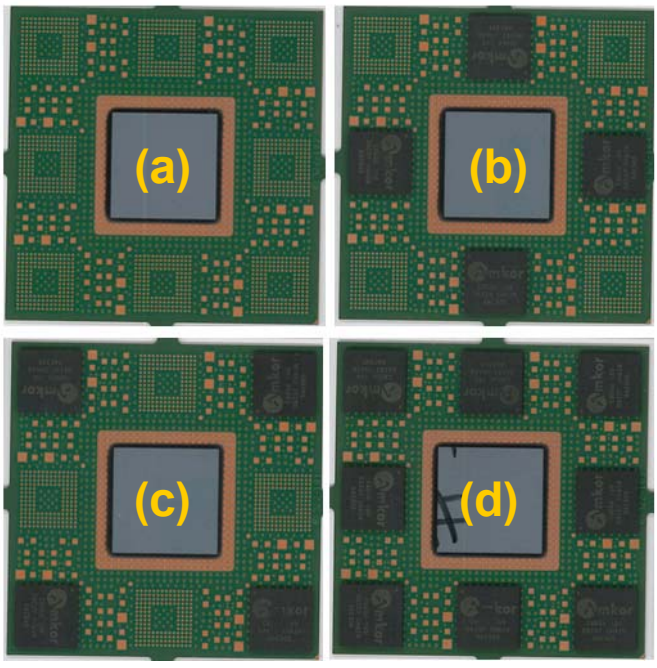
A FINEPLACER Pico ma research die bonder is now operational in the Advanced Process laboratory. The Pico bonder places devices with a 5µm X-Y positional accuracy and supports up to 700N bonding force. It has separate top and bottom heating units for control of the through thickness temperature gradient during the bonding process. The APL bonder additionally includes a multiple depth flux dip tray and a precision Z-position stop for controlled bond line thickness. It has been initially outfitted with heated pick tools appropriate for either small die (3 – 5 mm) or large die (12 – 16 mm). Others will be acquired as our die attach research activities demand.



REL17A. System in Package Interconnect Reliability – SAC305

Product designers are systematically migrating more and more function from the motherboard surface to highly integrated System in Package (SiP) structures. This increases the product functional density of course but the reliability consequences are often uncertain. This project compares the interconnect reliability of a 12x12 mm molded CSP memory package (0.8mm pitch) when positioned on a large laminate (SiP) substrate relative to what is had been with its conventional placement directly on the motherboard.

Two 60 x 60 mm ball grid array System in Package (SiP) components have been designed for reliability test. Set-up samples of candidate structures have been fabricated for dynamic warpage analysis. Each SiP device contains a central, underfilled, 20mm integrated circuit which can be flanked by up to eight daisy-chained CSP memory devices. The SiP test components have been fabricated with two different I/O counts and BGA pitches; one design containing a 45x45 array at 1.27mm pitch and the other design containing a 58x58 array at 1.0mm pitch, both using SAC305 solder balls.



Four CSP placement configurations have been selected for study. These will be repeated for both SiP I/O pitch parts:

a) no topside memory devices
b) edge placements
c) corner placements
d) edge and corner placements

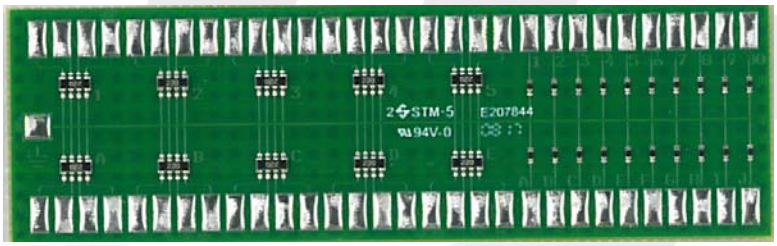
Additional samples will be fabricated and reflow soldered to motherboards for thermal cycle reliability test in a -40 to 125°C environment. Event detection will monitor the electrical integrity of the SiP BGA interconnections and the SiP mounted CSP memory device interconnects relative to those of control memory devices placed conventionally on the motherboard surface.

REL9A. Via in Pad Plated Over (VIPPO) Soldering Defect

The bill of materials for the VIPPO solder defect test board is nearing completion. Several well-known component suppliers will be contributing testable parts ranging from a 13.5mm CSP to a 55mm PBGA. In the meantime, mechanistic experiments with single solder joints are underway to identify conditions under which this characteristic solder defect can be created. The technique generally involves applying a tensile force smaller than the joint strength to single-joint "assemblies" while increasing their temperature until a separation occurs. The intent is to reproduce a VIPPO-type failure surface. The heating can be applied isothermally or with a controlled temperature gradient across the soldered interface. The latter approach has been used to date to produce interfacial failures similar in appearance to VIPPO defects. The separation was at the component pad intermetallic level, as in the VIPPO cases, but with a small amount of solder still detected on the component pad IMC. The technique is still being refined.

MAT8. Variability in Sulfur Induced Resistor Corrosion Response

As a peripheral study to our ongoing evaluation of sulfur corrosion mitigation by various conformal coatings, we are also examining the variability in corrosion sensitivity among the device finishes available from various resistor suppliers. The corrosion test coupon designed for this investigation is assembled with thick and thin film RNET and 0402 resistors. The coupon will not be conformal coated; rather it will serve to evaluate differences in corrosion response due to the subtle variations in surface finishes available from various suppliers.

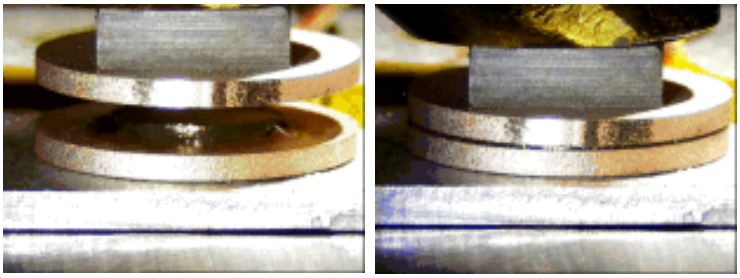


RNET and 0402 coupon for surface finish corrosion sensitivity comparison.

MAT6C. Sintered Silver Die Attach

A new sintered silver paste that includes nanometer-scale silver particles was acquired and evaluated for pressureless sintering. A wide range of sintering conditions and environments were examined using the APL Finetech FINEPLACER® Pico bonder for placement and heating. After sintering, large gaps of various shapes and sizes often spanning the entire bond line were always observed inside the silver joint. These gaps should have a detrimental effect on both bond strength and conductivity compared to the micro-scale paste used in prior experiments.

A technique to measure the effective thermal conductivity of sintered silver joints has been developed and used for both the nano- and micro-scale pastes. As expected, the thermal conductivity of the gap-free micro-paste was much higher than that of the nano-paste, although still only a fraction of the conductivity of solid silver because of the porous nature of the sintered joint.



Silver paste deposit between two copper disks being prepared for conductivity measurements.
Left image: During placement
Right image: After placement

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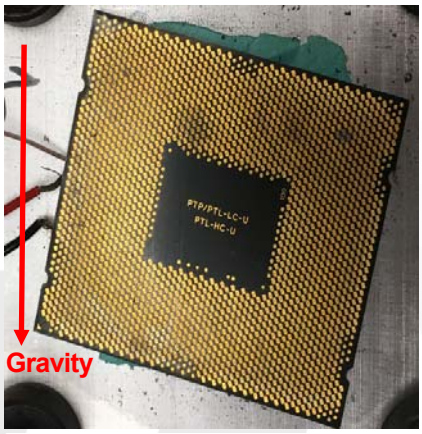
MAT4B. Component Level Testing of Thermal Interface Materials

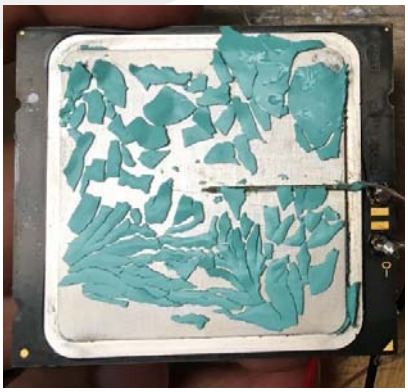
Component level thermal (CLT) testing has been completed on several latest generation thermal interface materials (TIM) designed for use between a lidded chip module and an aluminum heat sink. Thermal performance stability in accelerated thermal cycling from -40 to 125°C was evaluated for three such thermal putties: two silicone based and one non-silicone formulation. The CLT fixture was used in a fixed gap mode, with no spring pressure. Using electrical capacitance methods, TIM bond lines were measured to be 0.4 mm. Measured time zero thermal resistances were on the order of 200°C mm^2/W. Fixtures were oriented so that the TIM plane was vertical during the thermal cycle to investigate the effect of gravity on unconstrained heat sink attachments.



Above: Motion of thermal test module after thermal cycle exposure.

Below: Aluminum heat sink and thermal test module mating surfaces separated after thermal cycling.

During thermal cycling, cyclic strains induced by CTE mismatch can degrade the integrity of TIM layers. Typical and significant movement of the thermal module relative to the aluminum heat sink that occurred for the two silicone thermal putties is shown at right. Separating surfaces after test revealed cracks and fissures in the TIM as well as areas of missing material. While thermal putties have some structural integrity due to their low cross-link density, adhesively, they are very weak (<0.03 MPa) in shear. Therefore, to prevent relative movement between the thermal module and heat sink, mechanical retention is required. However, even with mechanical retention, the cracks and fissures in the TIM will still occur. The combination of the physical movement and damage in the TIM that can be seen after separation, explains the 38 to 75% increases in thermal resistance observed for the two silicone putties. In contrast, the non-silicone thermal putty exhibited stable thermal resistance throughout thermal cycle testing with no discernable movement and negligible physical damage in the TIM after the test. Caution is still warranted in using this non-silicone thermal putty and long term, application relevant thermal aging studies are needed to fully assess its stability. Low cross-link density non-silicone TIMs are known to oxidize during long term temperature aging and become brittle.



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Additions to the AREA report archive …

Effect of Low Volume Solder Paste Deposit Outliers on BGA/CSP Assembly and Reliability Expectations
by Sai Sriperumbudar, Martin Anselm and Michael Meilunas

Thermal Cycling Reliability of Underfilled Assemblies on TB2013
by Pericles A. Kondos