AREA Consortium

Dear Members,

We've just completed the mid-year consortium meeting earlier this week. We do appreciate your participation in these events. Thank you. The agenda included the usual reviews of key research activities but we also allocated a little time to discuss a few potential new research thrusts.

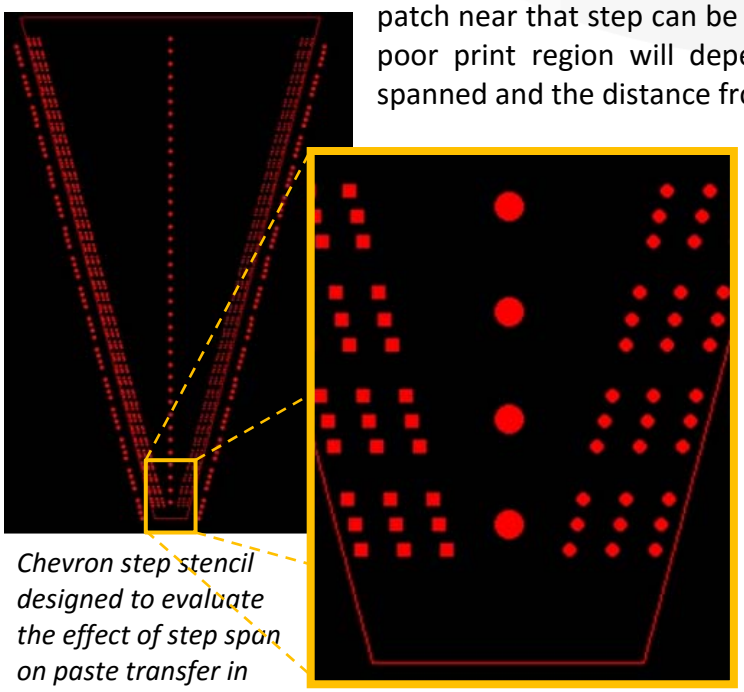
With our newly acquired capability for efficient measurement of TIM thermal resistance, we're exploring ideas for meaningful research on TIM2 processing and reliability. Second, we have been putting some serious thought into how to best select a failure detection system for the various reliability tests that we routinely run in our lab. Under what conditions is it advantageous to use resistance data loggers vs. event detection systems? Should joints with compressive loading (*i.e.*, underfilled, conformal coated, heat sink compression, etc.) have a different monitoring protocol than bare components? How do you best capture failures in dynamic systems (*e.g.,* vibration, drop/shock)? Analysis Tech (maker of our event detectors) has agreed to introduce some software changes to address at least a few of our concerns. If you have a reliability testing challenges with uncertain failure detection criteria and would like offer up a case study, please contact Mike Meilunas, <meilunas@uic.com>.

Sincerely,

Jim Wilcox
Consortium Manager

APD1A. Broadband Solder Paste Printing

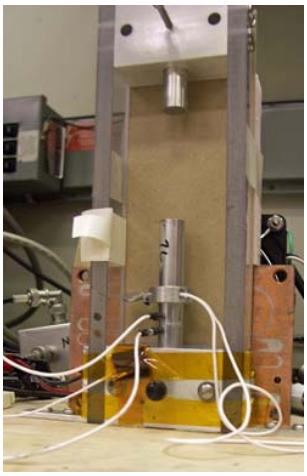
The broadband printing project has been exploring the limitations of printing fine feature paste deposits in close proximity to coarse feature deposits. This is often accomplished through the use of thinner (or stepped) patches of the stencil in the fine featured region. Paste printing trials were completed with 120µm stencil having both 100 and 75 µm thick patches. Successful integration of the 75µm patch was a bit more difficult than the 100 µm patch but good results were achieved by increasing the print squeegee pressure. Because the print squeegee must bend to accommodate the physical step at the edge of the patch, paste deposits within the patch near that step can be of questionable quality. The size of the poor print region will depend on the width of the patch to be spanned and the distance from the step.



Chevron step stencil designed to evaluate the effect of step span on paste transfer in close proximity to the step edge. Print direction is vertical.

Through the use of patches with gradually changing width, both the patch width and the distance from the step edge to an aperture were found to be important in determining print quality. For example, the 75 µm thick patch at a 13mm width required a minimum 1.8mm step edge to aperture distance to ensure consistent solder paste deposition. This and other step edge to aperture limits identified in the study align well with current IPC recommendations but the patch width contribution had not been previously addressed.

MAT4B. Thermal Interface Materials Studies



Protocol for the characterization of thermal interface materials has been defined and capability is being established in the Advanced Process Lab. Important characterization methods include measuring unit area thermal resistance, effective thermal conductivity, rheological behavior and dynamic mechanical properties. These methods are used at both time zero and after environmental stressing to establish a base line thermal performance and to understand long term stability. The baseline thermal resistance method has been demonstrated with several materials of interest provided by the consortium membership. We are soliciting application and process research suggestions from Consortium members. Investigations are expected to address materials defined for use with package level thermal interfaces (TIM2).

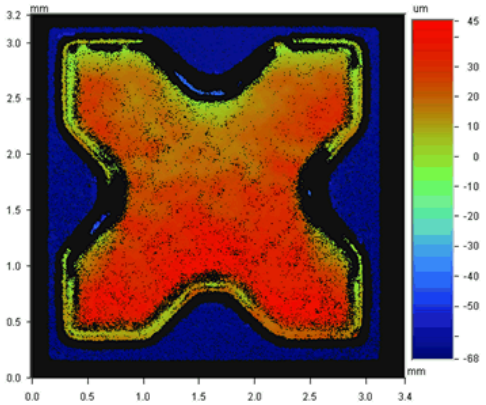
MAT1B. Reworkable Component Underfills

Thermal cycling of TB2014U boards was concluded and the remaining assemblies were removed from the chamber. Planned pad strength tests in all combinations of reworked assemblies (cycled and non-cycled, underfilled and non-underfilled) for all four underfills as well as of never populated or cycled pads have been performed. Results are being analyzed. The strength response of pads on cycled underfilled boards was rather unexpected but consistent for all four underfills.

All TB2015 assembles have been underfilled and cycling has started, without any failures to date. New boards populated with large BGAs (928 I/O) were acquired from a consortium member, together with four untried underfills. Underfilling of the components is almost completed and ATC testing will commence soon. The planned treatment for these boards parallels that of TB2014U (cycling, reworking including underfill removal, pad strength testing).

MAT6B. Sintered Silver Die Attach

A modification in the stencil design allowed the use of paste printing instead of manual dispensing as a way of depositing silver sintering paste on substrates. Sintering trials have been run at various temperatures and sintering atmospheres. Changing the sintering temperature was found to produce acceptable bonding on metallizations that had not worked earlier. In contrast, the atmosphere had little effect on bond strength but did have a large effect on pore/particle sizes after sintering. Aging studies were performed to study the effect of long-term high-temperature storage on the shear strength of the die. A thicker stencil was used to create and test assemblies of a thicker bondline.

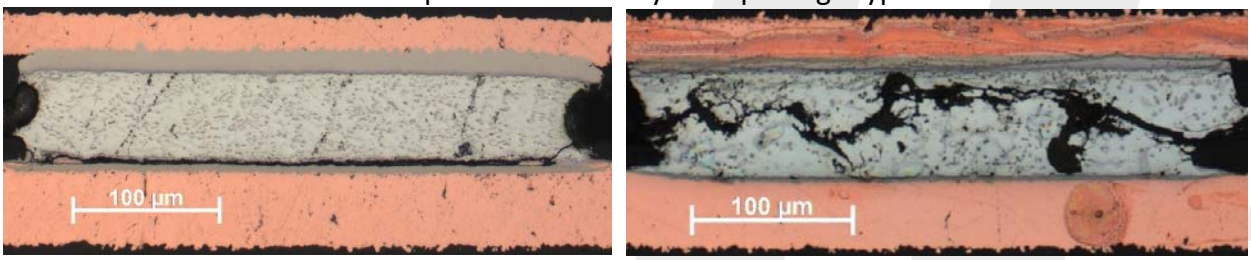


Gradations in silver paste print deposit height as measured with the WYCO profilometer.

MAT7E. Alternate Solder Alloy Effects on Thermal Cycle Reliability

ATC failure rate data collection for the alternate alloy project is nearing completion for most package types although some smaller packages have yet to produce many failures at all. Comprehensive microstructural analysis of the various solder alloy joints is progressing. The effort includes detailed characterization of the Sn grain and second phase particle morphologies as well as comparisons of the as-reflowed structures with those formed after extensive thermal cycling.

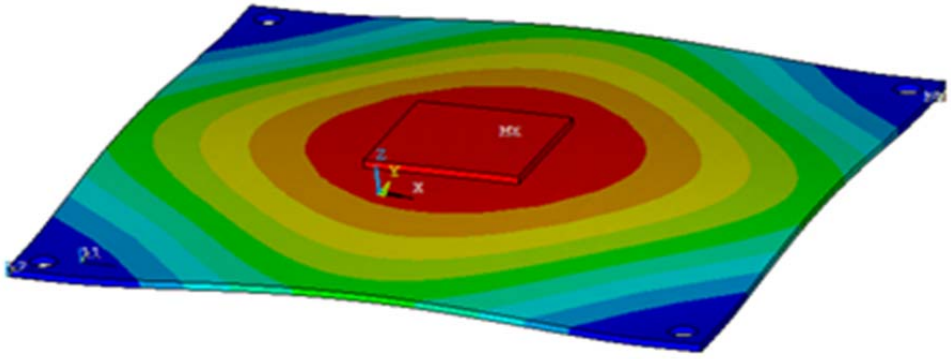
A systematic analysis of failure modes reveals some interesting correlations. With identical component finishes and board finishes, solder joints in the CALGA256 package typically fail on the board side while in the CALGA/BGA208 packages the same solder alloys fail on the package side. Interfacial failures are far more prevalent in early life failures as shown below for one experimental alloy. Other failure modes were also observed; pad cratering for instance, which tended to be confined to specific solder alloys and package types.



LEFT: An experimental alloy solder joint with an interfacial separation along the ENIG board finish that produced an anomalously early ATC failure. RIGHT: A much later failure on the same ENIG board clearly arises from solder joint fatigue.

REL3C. Elevated Temperature Vibration Testing

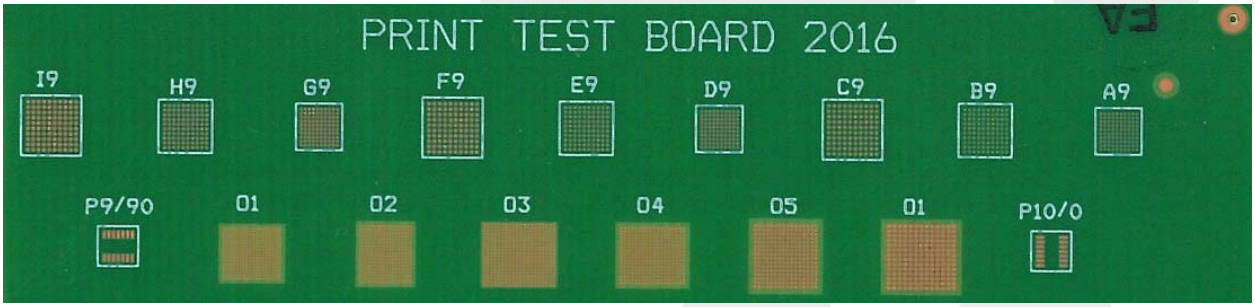
Elevated temperature vibration testing of SAC305 BGA connections continues. Reliability tests have been run with forced harmonic accelerations between 0.3g and 3.5g to produce solder joint failures in the corner joints of a single BGA208 package. Test temperatures of 25C, 80C and 120°C were used. Clear correlations have been found between the vibration induced board deflection and cycles to failure. The sensitivity of solder joint cyclic life to the imposed board deflection decreases with increasing temperature. Room temperature vibration showed the greatest dependency of cyclic lifetime on board deflection. Further analysis is underway to identify the functional relation between board deflections and solder joint cyclic strain.



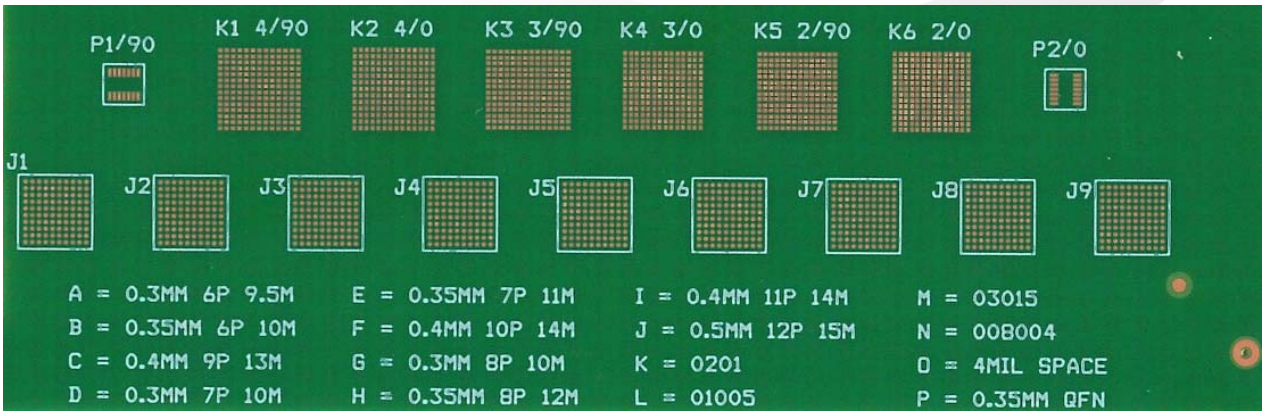
First mode shape during natural frequency vibration of the VTV test board. Area of maximum deflection at the component site imposes cyclic solder join strains and subsequent failure.

Fine Pitch Solder Paste Printing

Printed circuit board assemblies for handheld, consumer electronics are characterized by very low profile components placed on thin boards with extremely high density. These designs requires very fine pitch, high resolution solder paste printing. We are exploring the limits of this process parameter space with our newly received Print Test Board 2016.



This 0.6mm thick board design contains 0.3, 0.35, 0.4 and 0.5mm pitch CSP footprints as well as 01005, 03015 and 008004 passive placement sites. The components are strategically arranged for solder paste printing experiments with a focus on stencil technologies. Several stencils have already been acquired for the project, including an 80 micron thick fine grain stencil, 50 and 80 micron thick stencils with Nami nanocoating and 50 and 75 micron thick stencils with DEK Nano Ultra coating. Other variables to be investigated include aperture shape and size and solder paste material. We are currently in the process of programming and validating our solder paste inspection (SPI) routine and will begin printing trials shortly.



Upper and lower board edge segments of the Print Test Board 2016 enlarged to show fine pitch features.