Dear Members,

The first order of business this month is to congratulate our prolific graduate research assistant, Mohammed Genanu, of the Binghamton University Physics Department. He was recently recognized by the SMTA for the Best Student Paper at the recent SMTA International conference. There he presented some of his consortium research on fine pitch copper pillar interconnects. His careful work was executed mostly here in the APL with the active participation of his academic advisor and our longtime collaborator, Professor Eric Cotts. Of course if you attend our meetings, you get to see this world class content routinely. His handiwork was featured prominently in the recent October meeting; including comparisons of conventional and laser reflowed Cu pillar interconnects.

The award is an indication of the quality of the research we get from our academic partners. It also offers me an opportunity to highlight the ongoing partnership that our consortium has with academia. Each year, a number of our research projects are done in direct collaboration with select faculty and students. The object is always to maintain a balance between the industrial relevance of our work and the scientific understanding of the phenomena in question. We will continue to establish these cooperative academic partnerships in key areas of interest to our members, reaching out to relevant universities as our portfolio demands (and our budget allows).

Sincerely,

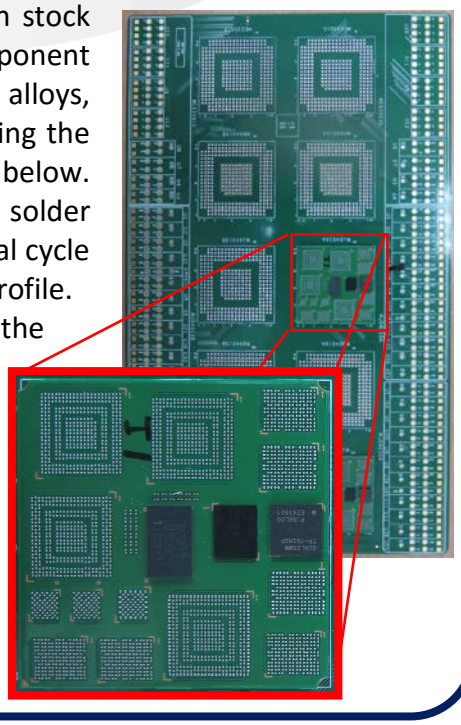
Jim Wilcox
Consortium Manager

REL17A. System in Package (SiP): Mixed Solder Assemblies

Consistent with the industry drive for ever denser heterogeneous packaging integration structures, AREA members are showing interest in evaluating System in Package designs. To that end, testing is underway on the interconnect reliability of some simple SiP building blocks: CSP and WLCSP devices on a laminate substrate. The test vehicle was provided by a member who is exploring alternate alloy solder pastes. The SiP structure includes a 5.8x5.8 mm CSP and a 5.97x4.82mm WLCSP device, both with continuity test nets. A third WLCSP is not testable.

The two 0.4mm pitch testable devices were sourced with stock solder balls, either SAC124Ni or SAC405 composition. Component attachment however was done with two candidate paste alloys, Innolot and Senju M794, along with a SAC305 control producing the twelve package/mixed solder alloy combinations tabulated below. SiP structures were soldered to the test board using SAC305 solder preforms and paste. Assemblies are now in accelerated thermal cycle test with a -40 to 125C profile. Initial results indicate that the SAC405/M794 combination performs measurably better than the other five alloy combinations.

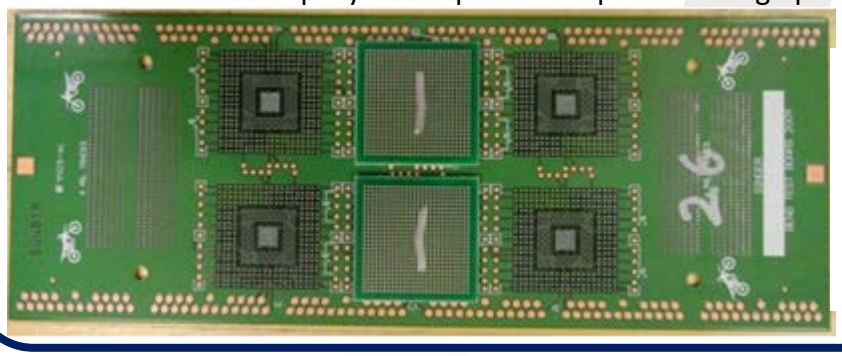
CMP	Solder ball	Solder paste
CSP	SAC125Ni	Innolot
		M794
		SAC305
	SAC405	Innolot
		M794
		SAC305
WLCSP	SAC125Ni	Innolot
		M794
		SAC305
	SAC405	Innolot
		M794
		SAC305



SiP emulation structures: three fine pitch packaged devices on a 1.5mm thick substrate joined to a 1.5mm thick test board.

Cyclic Pad Cratering Resistance of PCB Laminates

A cyclic 4-point bend test was utilized as a means for evaluating pad cratering fatigue resistance of five PCB laminate materials. An existing consortium test board design was fabricated using various different laminate materials: Nelco 4000-13, Nelco 4800-20, MeteorWave 1000, ISpeed, or ZetaCap over Megtron IV. Two large pitch BGA dummy components were soldered to the centerline of each board and the assemblies then subjected to a cyclic 4-point bend test to stress the soldered connections and underlying pad/laminate bond. Repetitive board bending was performed at a displacement rate of 10 mm/s. Board surface strain and strain rates were measured on representative setup samples. The onset of pad cratering during cycling was detected by monitoring the electrical continuity of surface layer traces on the PCB near the high stress BGA solder joints. Cycling beyond initial failure detection was routinely performed in an attempt to drive measurable pad cratering. Subsequent data analysis would indicate that the samples containing the ZetaCap layer withstood significantly more cycles before electrical failure than the other laminate materials. Failure analysis would confirm that the ZetaCap layer also prevented pad cratering up to 8000 bend cycles.



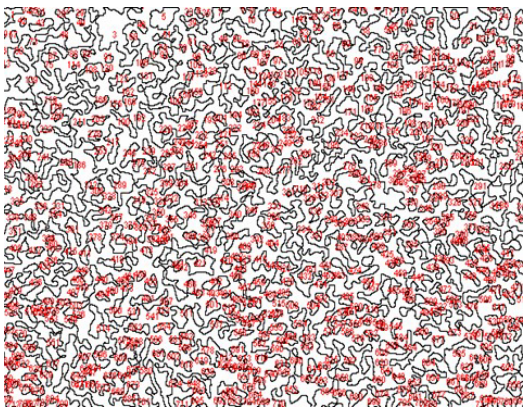
AREA Consortium 4-point bend test board design (rev 1) used for this cyclic pad cratering study.

Two dummy BGA components are attached along the vertical center-line which serves as the bend axis.

MAT6B. Sintered Silver Die Attach

Long term aging of sintered silver assemblies at 220°C is underway. An earlier aging experiment at 250°C failed to test the sintered connection. After 1000 hours, die shear testing mostly produced failures in the substrate dielectric layer (under the Cu pad), indicating that the T-clad substrates are not stable at 250°C. Even so, some 250°C aged samples did fail in the joint, providing intriguing information regarding the changes in strength when sintered silver joins two Ag surfaces or two Au surfaces. Although not conclusive because of the small number of valid joint failures, the evidence from the 250°C aging suggested very different behavior of the bond formed to a Ag finish compared to the bond formed to a Au finish. The present reduced temperature aging run further includes samples with Ag on one side and Au on the other.

In other processing evaluations, the effect of lowering the sintering temperature on the strength of the bond at a Ag finish interface was studied relative to that at a Au finish interface. Finally, sintering on Au pads at 250°C in nitrogen instead of the previously used air atmosphere was found to produce very different results in both strength and microstructure. Porosity measurements have been made to quantify the effect of sintering conditions (temperature and atmosphere) on the porosity and average pore size.

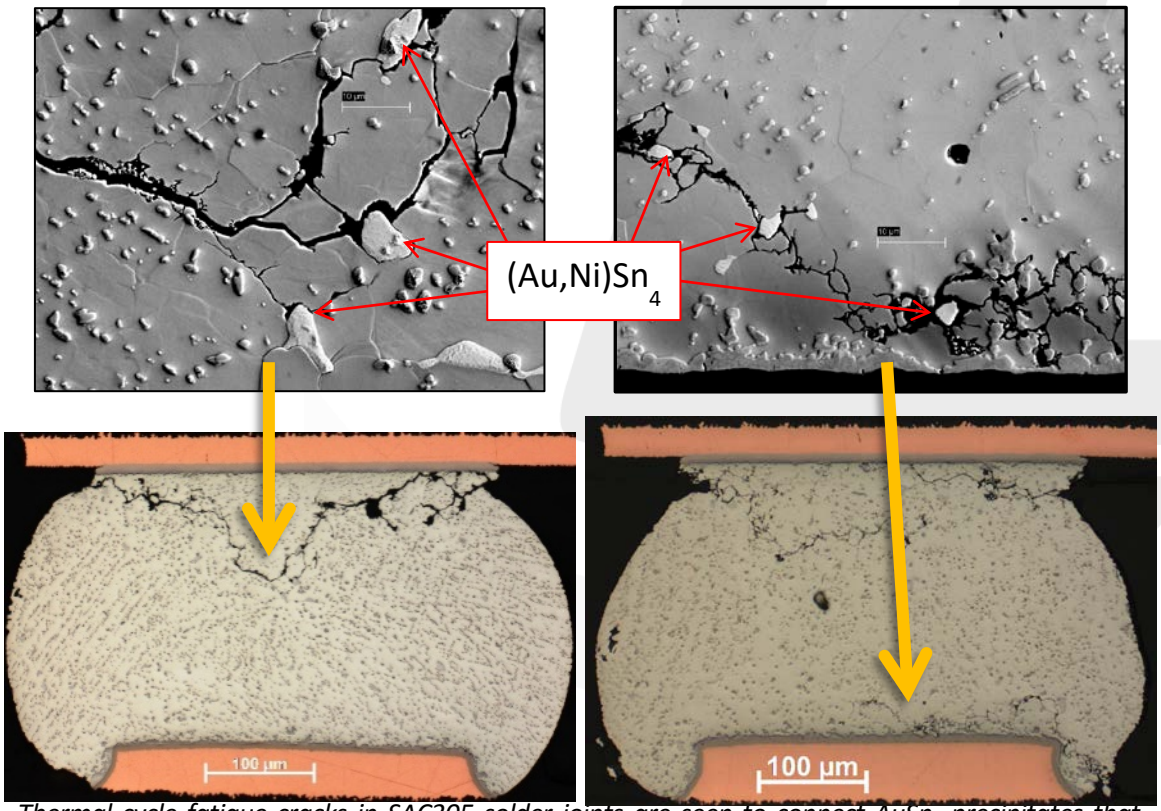


Digital rendering of sintering porosity with void count.

MAT7E. Surface Finish Effects on Thermal Cycle Reliability

When Ni finished BGA components are soldered to an ENIG finished board, no Cu is dissolved into the joint minimizing the formation of Cu_6Sn_5. The additional dissolved Au however forms $AuSn_4$ precipitates. On thermal cycling to failure, solder fatigue cracks often connect a string of these $AuSn_4$ particles. Perhaps not surprising, since thermal fatigue cracks in SAC solder are known to follow recrystallized Sn grain boundaries and such Au precipitate particles pin the moving Sn boundaries and so necessarily reside on those same boundaries.

Interestingly, these particles at the recrystallized Sn grain boundaries may moderately inhibit the propagation of cracks along these boundaries. The ATC characteristic life of the BGA208 component for instance is 15% greater on an ENIG board where such $AuSn_4$ particles are present than on an OSP finish board which produces no $AuSn_4$ particles in the solder joints.



Thermal cycle fatigue cracks in SAC305 solder joints are seen to connect $AuSn_4$ precipitates that characteristically form when soldered to an ENIG board finish. Early fail (LEFT) and late fail (RIGHT) from the failure rate distribution of a BGA208 device in a -40 to 125C thermal cycle.

MAT1B. Reworkable Component Underfills

Two distinct underfill studies are in progress. The second study uses four different underfills on TB2016U with four populated sites per board, all with a large BGA (40mm x 40mm, 928 I/O). These boards have now exceeded 2000 cycles ATC. Two underfill sets have failed completely and have been removed from cycling. One of them was a non-filled reworkable underfill but, surprisingly, the other early failing material was highly filled. It was the only non-reworkable material included and so had been expected to perform quite well in ATC. A full rework process study of the three reworkable underfills will proceed shortly. It will investigate the ease of component and underfill removal as well as identify any visible or latent damage to the circuit board laminate, analogous to the similar underfill study previously done on TB2014U.

REL15C. Superimposed Power Cycle and Thermal Cycle Testing

Traditional thermal cycle testing of electronic hardware in an environmental chamber has been supplemented with power cycle testing. The intent of this project is to provide a more realistic approach to thermal mechanical reliability stressing through the inclusion of transient temperature gradients similar to those produced in the field operation of functional electronics. In some field applications, hardware is housed in unconditioned structures and can therefore experience diurnal thermal cycling with seasonal temperature extremes. A recent interest in the electronics reliability community has been the combination of environmental thermal cycles with mini-power cycles. Through collaboration with other industry groups, we have obtained the flipchip PBGA test samples necessary for such work. This test part is a 45x45 mm laminate BGA package attached to a printed circuit test card. The test package contains a 15.4 x 15.8 mm flip chip with a main heater for uniform heating as well as three local individually controllable "hot spot" heaters and five temperature sensors. The BGA solder joints along the package perimeter and those beneath the flip chip comprise five electrical continuity test nets to be monitored for failure during the combined cycling.

Our custom designed power cycle test circuit is used to supply a constant current that drives the main chip heater at the time intervals of interest. It further monitors for short duration resistance 'events' and records analog voltage drop on each net to monitor changes in the net resistance, providing a comprehensive failure detection system for every part on test.

Testing of eight such modules has begun using an environmental thermal cycle of -40 to 90 C, (135 minute period) and a +30 C mini power cycle (15 minute period), superimposed asynchronously. The plot below shows the actual chip temperature as measured by on-chip temperature sensor #1 (blue) that is located between the center of the chip and a midpoint of an edge. The red line is the programmed temperature profile for the environmental thermal chamber.