AREA Consortium

Dear Members,

Descriptions of our planned research activities for the coming year have been formalized in the 2016 Research Plan. Each project is described in the form of a brief technical abstract. You'll notice that some of the projects listed are continuations of multiyear research programs already underway. Other projects, newly defined from our annual member company consultations, are described simply as we currently envision them. Your planning input is still welcome. If an addition or modification to the experimental plan can make the results more relevant or valuable to your company please contact us: <jim.wilcox@uic.com>. As always, not all projects can be run in parallel. Some will necessarily start later in the year as we free up chamber space, test apparatus capacity or research staff bandwidth. Your participation is of course welcome in all projects regardless of their stage of execution.

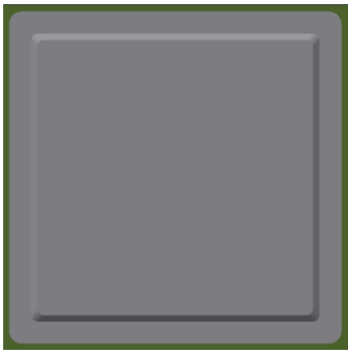
Deferring to common member preference, we are scheduling the first 2016 consortium meeting to allow a one week travel buffer after the IPC APEX meeting. That moves us out to March 30-31, 2016. We are planning a day and half itinerary of technical content at our usual Binghamton University campus venue. Mark your calendars.

Sincerely,

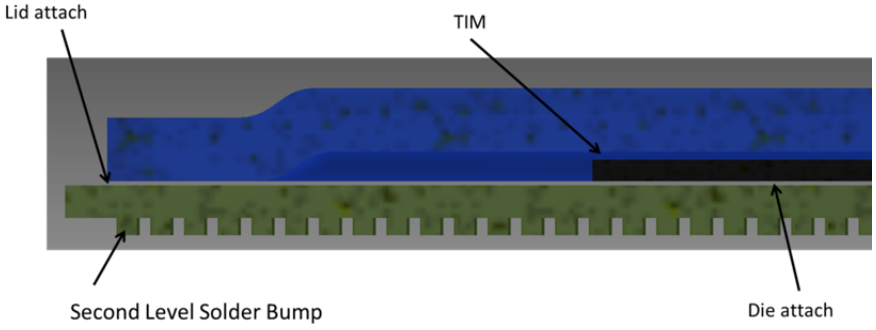
Jim Wilcox
Consortium Manager

**APD3D. Large Body BGA Characterization**

A new project is underway to evaluate the thermal cycling behavior of large body BGA components commonly used in enterprise server / telecom infrastructure applications. Limited data have been published on the reliability characteristics of such packages. Through collaboration with key AREA members representing that industry sector, a new test vehicle has been designed to evaluate the effects of die size, lid attach material and thermal interface materials on thermal cycle lifetimes. Warpage behavior of each package configuration during simulated reflow temperature will be characterized. The lifetime and failure mechanisms of assembled packages in a -40/125C thermal cycling test will be correlated to warpage measurements. Simulation work has begun to identify the contribution of various design selections on temperature induced warpage and in turn on interconnect reliability. Preliminary simulation results reported at the October meeting demonstrated that die size and mechanical properties of the thermal interface material significantly affect the warpage and stress levels on board level solder joints.



*53x53 mm BGA package with a coined copper lid.*

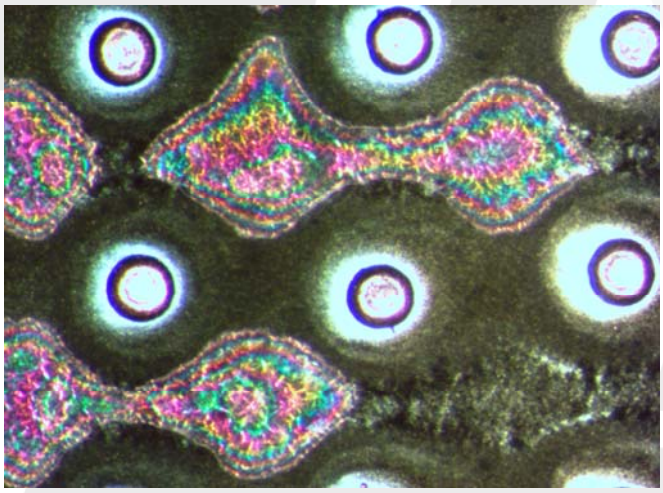



*Simulated cross-section of the large body BGA package to be tested. Build-up laminate substrates with a thin (600 μm) core are being used.*

**MAT1B. Reworkable Component Underfills**

Accelerated thermal cycling of TB2014U boards underfilled with materials G and H has begun and already several failures have been detected. Most of the boards of the older group (non-underfilled controls and materials E and F) have been removed from the ATC chamber. A small number of long lived components are still being cycled.

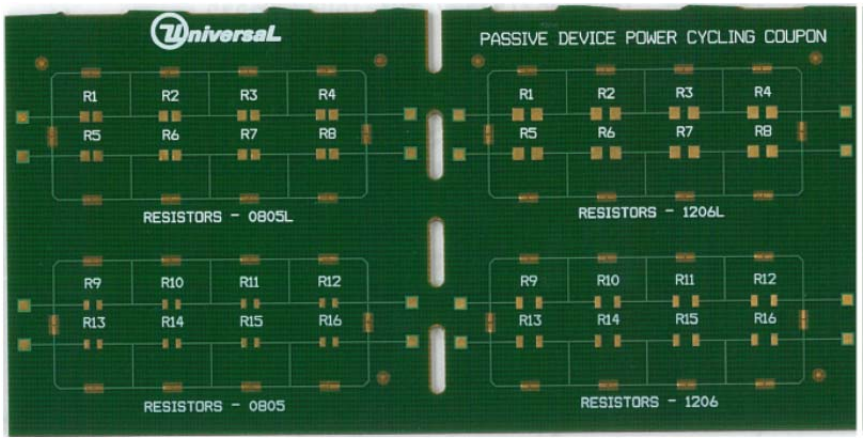
Programming of the manufacturing equipment for assembling TB2015U boards with Sn/Pb solder components is complete. In preparation for assembly and underfill, glass-slide flow experiments using the same underfills but with Sn/Pb paste residues have been conducted to determine the optimum underfill temperature. One of these materials, although unfilled, produced regions of two clearly different textures, one around the deposited solder bumps (where flux residues were located) and one in regions removed from the solder deposits. On cooling, shrinkage voids formed in some of these samples, following exactly the boundary between the two textures and limited to the between-the-rows texture. The conditions leading to larger number of such voids will be avoided during underfilling actual components.



*Regions of differing underfill textures visible among Sn/Pb solder paste deposits in glass slide flow samples.*

**REL15B. Power Cycle Reliability Test Method**

A method for reliability testing of board level interconnects using cyclically dissipated power through an induced current waveform is being developed using simple nets of surface mount resistors. Induced current waveforms will be defined to produce local heating to a predetermined target temperature. Two passive device sizes (0805 and 1206), assembled at the upper and lower design limits of solder joint volume, will be tested in a power cycle.

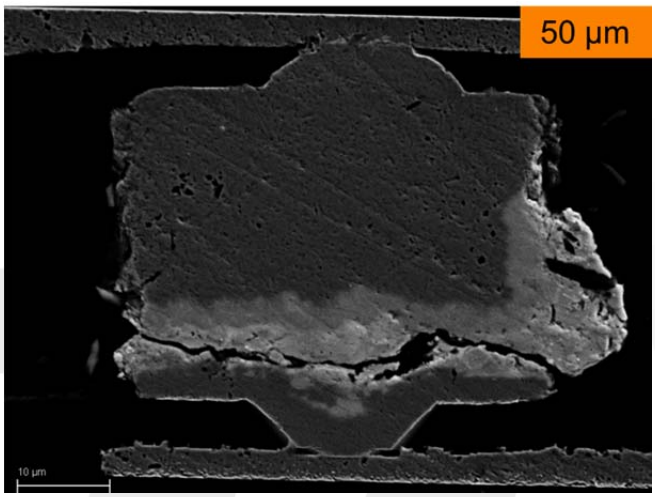



*Test board designed for power cycling of surface mount resistors. Different pad sizes allow for two solder volumes for each device size.*

Subsequent reliability testing using the method and apparatus defined above is planned for a 12 mm wirebond QFN package fabricated with a resistive element test die capable of producing either uniform heating or local hot spots. These parts are being assembled.

**REL12A. Fine Pitch Copper Pillar Interconnects**

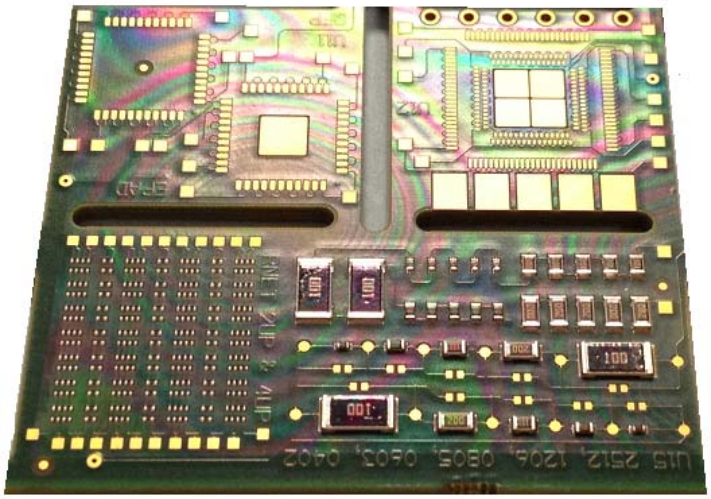
We continue to evaluate the reliability of fine pitch Cu pillar interconnects through accelerated thermal cycle and drop/shock testing. Initial results (limited sample) reveal that the underfill material and the choice of substrate material (*i.e.*, silicon vs. glass) can have significant effects on the lifetime of assemblies in thermal cycle. Careful microstructural analysis is in progress to understand the failure mechanism in these small joints containing only a limited amount of solder and compare to that of larger volume BGA solder interconnects.




*SEM image of a 50 µm diameter copper pillar assembled on a high CTE glass substrate that failed in -40/125C thermal cycle.*

**MAT8B. Conformal Coating Studies**

Reliability studies of the acrylic conformal coating materials Humiseal UV40 and UV50 are nearing completion. Most components have failed or are nearing their ATC lifetime. Results will be reported at the March meeting. These coatings are generally thick relative to the standoff of most components on the board and are known to affect the solder joint reliability of package types used for active devices. Some alternate coating materials, such as Parylene or the new plasma nanocoatings, are inherently thin relative to package stand-off heights. Without filling the under-package gap such thin coatings presumably would impart little thermomechanical stresses to component solder joints. They may however still produce a similar effect on very low standoff passive devices. Impacts of thin coatings to the thermal cycle reliability of SMD passive devices (in our case, resistors) are being investigated. SMD resistor array coupons on the TB2015 test board have been coated with either Parylene C or Semblant SEM400 nanocoating and are now being wired for thermal cycle testing of the passive solder interconnects.



*Thin film interference patterns arising from the ~micron thick Semblant SEM400 plasma nanocoating. Coated resistors to be tested are visible in the lower right coupon.*